Seven Level Inverter LCL Filter

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Abstract:
The paper presents the controlling of current in single phase grid connected seven level multiinverter with boostup operation. Here we get output as 1.5 times of input using charge pump principle with less harmonic distortions. By using LCL filter we can control the current which removes the LCL resonance and maintain the stability at different load conditions. By using SPWM we can drives the switches, and also the capacitors balance is the main aim of the switching pattern.

Index Terms: LCL filter, Multilevel inverter, SPWM, Current control.

I.INTRODUCTION

The 3-Level inverter has some drawbacks such as non-reliable operation, filter design, and switching stress. Various levels of inverters are needed in high-power applications to meet the requirements. A multilevel inverter generates output voltage in the form of a staircase while improving power quality and conversion efficiency [1]. Voltage balancing is crucial, but so are component counts, driver circuit sizes, and capacitor counts as the number of levels increases. [2]

There are three different topologies for multilevel dc–ac converter that use IGBT switches. The panel's terminal voltage in grid-connected photovoltaic (PV) systems is low and fluctuates depending on the environment conditions.

The efficiency and power density cannot be maintained by the boost converter alone; however, more power density and more efficiency can be achieved without the need for an inductor by employing a capacitor charge pump.

Ten switches can be used in the design of a seven-mode inverter to boost voltage from the standard operating level to 3/2 times of the input[4], [5]. However, adding more switches raises costs and reduces efficiency.

Diodes are used in some seven level inverter, but usage of diodes, the inverters are impact the efficiency and do not meet the necessary voltage boost up level. By adopting a capacitor-based charge pump, the suggested multilevel inverter may increase the input voltage standard to 3/2 times of the input .

II.PROPOSED CONVERTER

Using seven modes, suggested multilevel inverter has the potential to increase voltage from 1.5 times its standard valueas illustrated in Fig. 4(a)–(g). The input voltage and output voltages are VD and Vo, respectively, and the input capacitors are C1 and C2. The input voltage can be shared evenly if the input capacitors are equal.

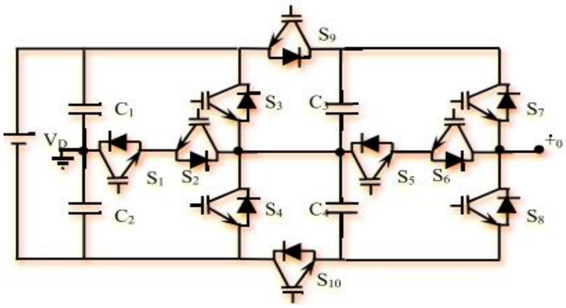
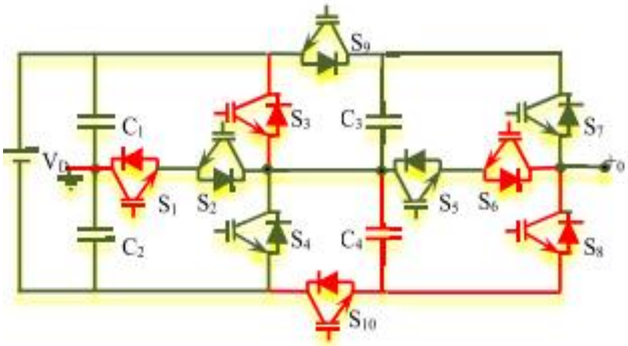


Fig.1.Proposedconverter

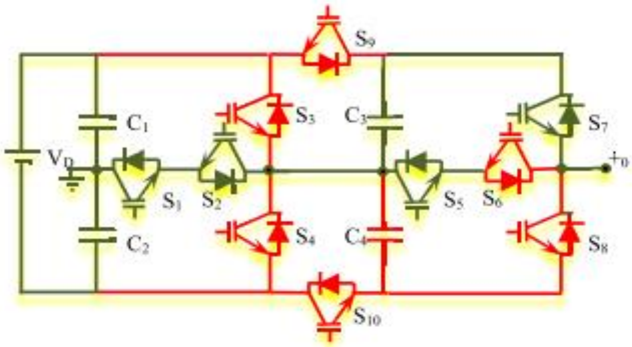
Two of the eight switches in the suggested architecture don't need antiparallel diodes. Since IGBT is the chosen switch in the proposed conversion system, only circuits can be extended to any level.

S 1	S 2	S 3	S 4	S 5	S 6	S 7	S 8	S 9	S 10	Voltage Levels
1	0	1	0	1	0	1	0	0	1	+1.5Vdc
1	1	0	0	1	0	1	0	0	0	+1Vdc
0	1	0	1	1	0	1	0	1	0	+0.5Vdc
1	1	0	0	1	1	0	0	0	0	0
1	0	1	0	0	1	0	1	0	1	-0.5Vdc
1	1	0	0	0	1	0	1	0	0	-1Vdc
0	1	0	1	0	1	0	1	1	0	-1.5Vdc

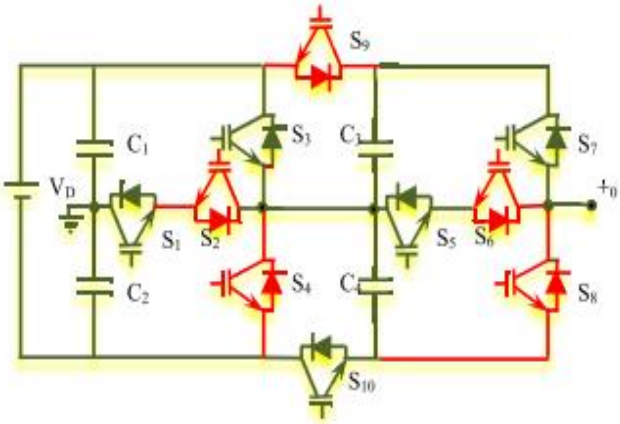
For Q4 and Q9 switches are turned on between 0.5 and -1.5 VD, floating capacitor C3 is charges to VD. At1.5 to −0.5 VD, the second floating capacitor was charged to VD. For each half of the voltage self-balancing action, C3 and C4 function symmetrically. C3 discharges through the neutral point or dc link capacitor during the positive half cycle, adding two more levels of voltage.C4 produces another half cycle voltages between −VD and −1.5VD.



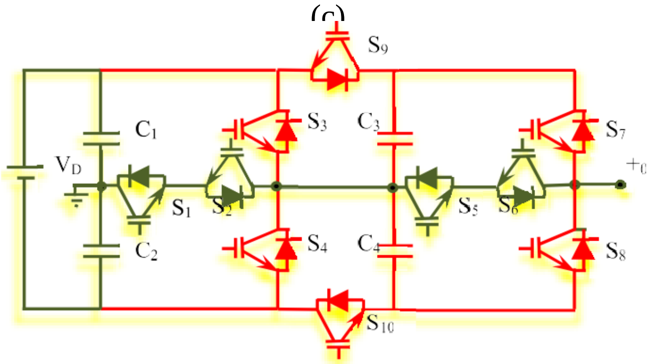
(a)


S_9
C_1
S_3
C_3
S_7
V_D
S_1
S_2
S_5
S_6
C_2
S_4
C_4
S_8
S_{10}

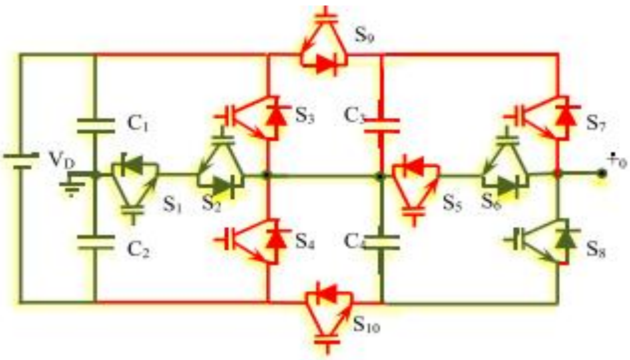
(b)


S_9
C_1
S_3
C_3
S_7
V_D
S_1
S_2
S_5
S_6
C_2
S_4
C_4
S_8
S_{10}

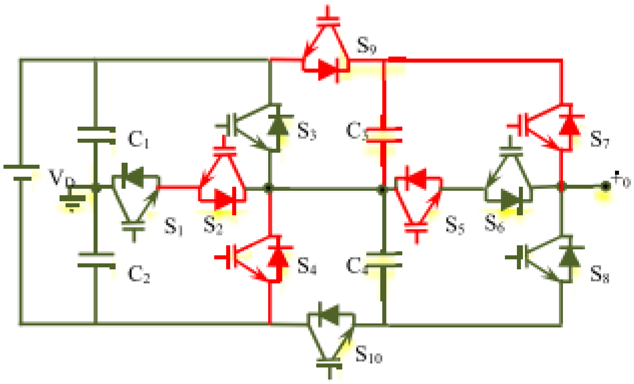
(c)


S_9
C_1
S_3
C_3
S_7
V_D
S_1
S_2
S_5
S_6
C_2
S_4
C_4
S_8
S_{10}

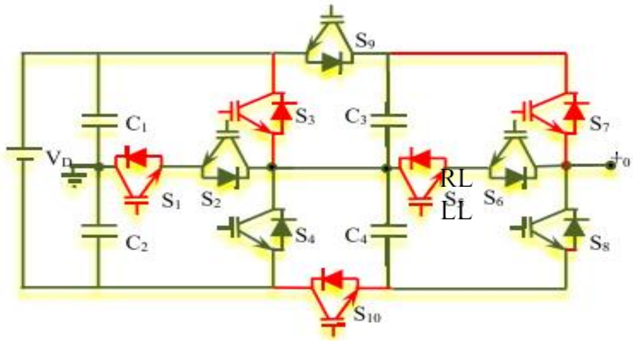
(d)


S_9
C_1
S_3
C_3
S_7
V_D
S_1
S_2
S_5
S_6
C_2
S_4
C_4
S_8
S_{10}

(e)



(f)

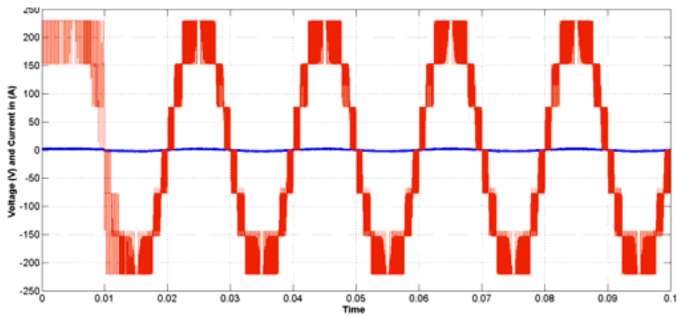


100Ω
0.1H
NJ40
CMF20120D

(g)

Fig.2.(a)I-Mode.(b)II-Mode.(c)III-Mode
(d)IV-Mode(e)V-Mode(f)VI-ModE(g)VII-Mode

Fig. 3. Seven level output



I. RESULTS AND CONCLUSION

Table II explains the specifications of the multilevel inverter and Table III explains the specification of Grid connected inverterter with LCL filter.Fig.4. illustrate the output voltage and output current with R load with 100 Ω.Here the output voltage follows the output current. From fig.5. explains the output voltage and current with RL load. Here the current is in sinuosoidal waveform because using a inductor. The inductor decreases the harmonic distrotions.The voltages and current of the multilevel inverter are shown for a load shift in Fig. 6. The 400 resistive load was attached to the load prior to the no load state. Lastly, an R-L load is connected to a load with a DC voltage and Frequency.

By varying modulation index (MI) at inductive load is shown in Fig. 7, We examine the output dc voltage and dc current for three distinct Modulation index values: 0.3, 0.6, and 0.9. The voltage levels of the inverter are maintained under this scenario, but the ±4Vdc width changes. This is similar to basic component variations, which are 100V, 200V, and 300V.

Parameters	Values
Input voltage Vi	100V
Fc	5KHz

Table II. Components Specifications

Parameters	Values
Grid Voltage	230v
Grid Frequency	50Hz
Grid side inverter	1.74mH
Filter side inverter	1.63mH
Filter Capacitor	15µF
DC Link Voltage	200v
Power	5kw

Table III. Specification of Grid connected inverter

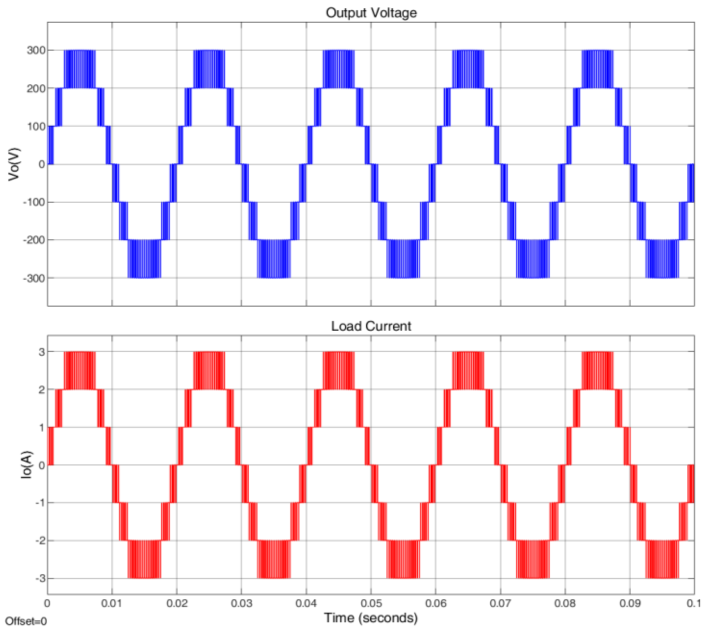


Fig.4 Output voltage and output current under R load (R=100Ω)

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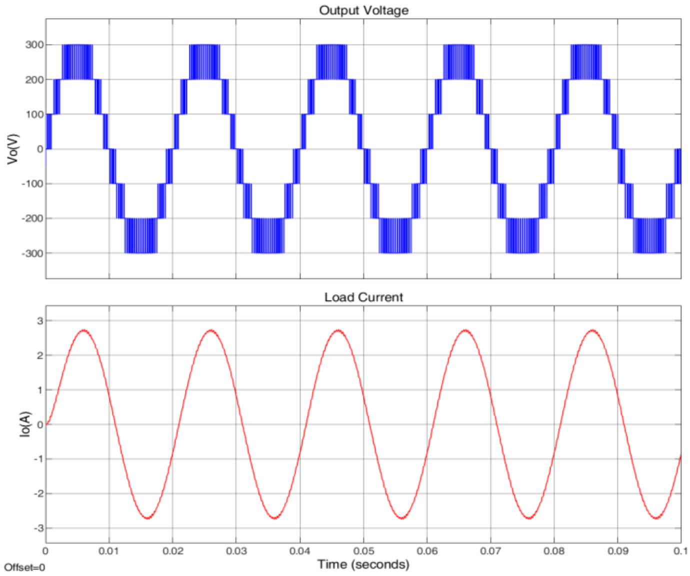

Fig.5: Output voltage and output current with RL load (R=100 Ω, L=100mH)

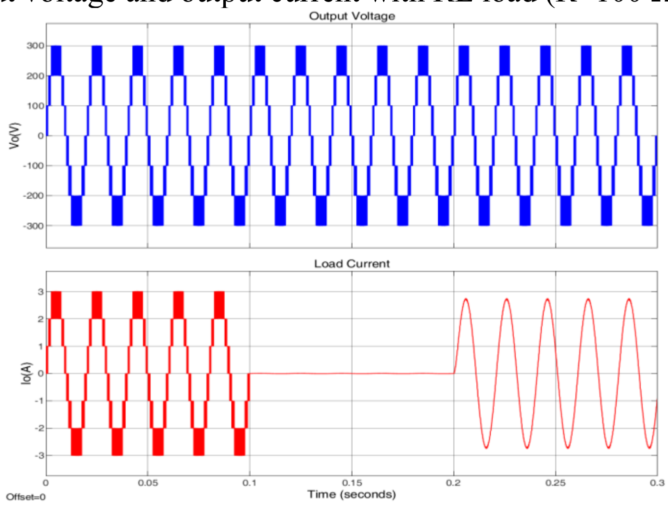

Fig.6: Output voltage and output current under dynamic load conditions (R=100Ω from t=0 to 0.1s, No-load from t=0.1s to 0.2s and R=100 Ω, L=100mH from t=0.2s to 0.3s)

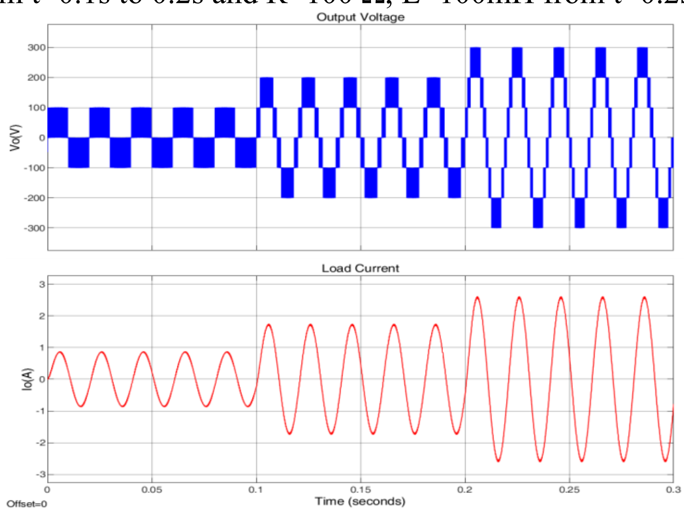

Fig.7: Output voltage and output current under variable MI conditions (MI=0.3 (3-Levels) from t=0 to 0.1s, MI=0.6 (5-Levels) from t=0.1s to 0.2s and MI=0.9 (7-Levels) from t=0.2s to 0.3s)

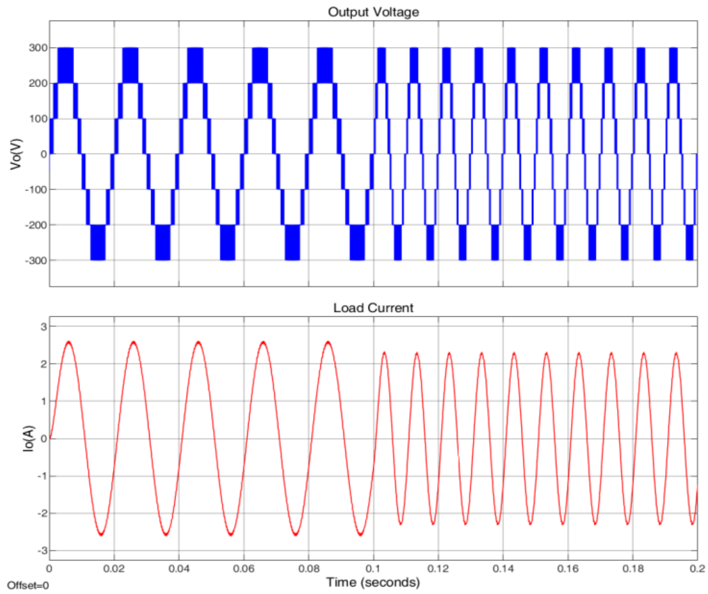

Fig.8: Output voltage and current under variable frequency conditions (f=50Hz from t=0 to 0.1s, f=100Hz from t=0.1 to 0.2s)

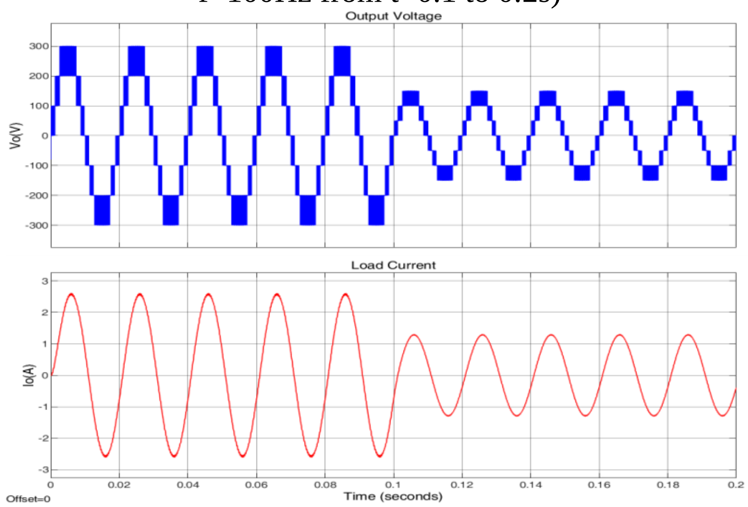

Fig.9: Output voltage and current under variable dc link voltage conditions (Vdc=200V from t=0 to 0.1s, Vdc=100V from t=0.1 to 0.2s)

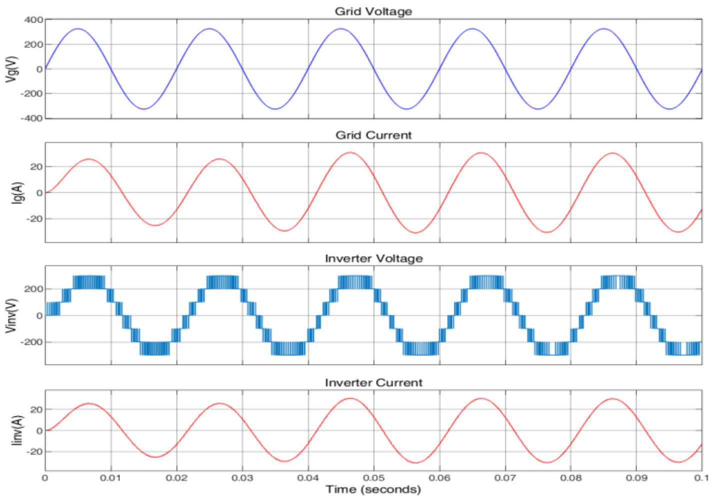

Fig.10: Full load condition Result

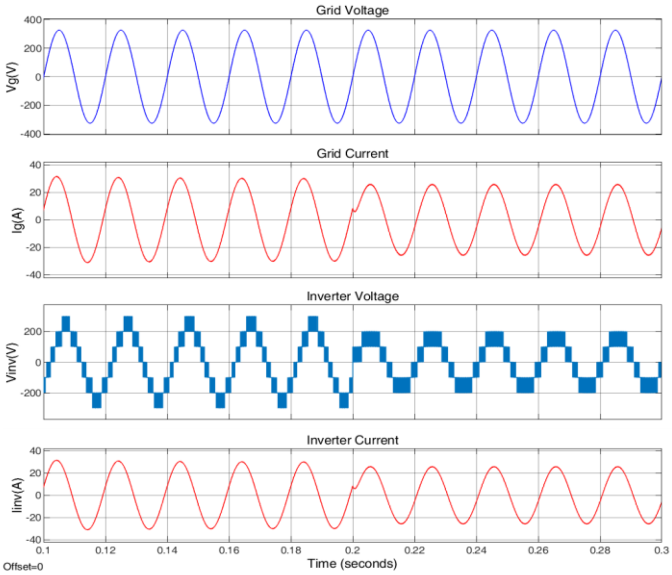

Fig.11: when current reference drop to 80% of full load current (from t=0.2s to 0.3s) from full load current (from t=0.1s to 0.2s).

Fig:8. Illustrate for different application we required different frequency.for example motor, we required different speeds,when frequency changes,speed also changes.For that at 50Hz , the timeperiod increases,as increasing the frequency the timeperiod decreases the current and voltage increases.
Fig:9.For different input voltage the different output current and voltage occurs.
In fig.10,Under full load circumstances, the grid voltage, and inverter side current are displayed. The injected current was eliminated and that synchronization and reference signal tracking are accomplished with the omitted steady state error.In fig11,examines the performance of the control approach by reducing the current from full load to half load settings.

IV.CONCLUSION

A current regulator for a single-phase LCL-filtered system has been demonstrated a connected seven-level multiinverter with boostup utilizing the charge pump method.The detailed operating modes of seven level inverterand circuit analysis are discussed.Here Switches are driven by SPWM, and the switching purpose is primarily utilized to balancing the capacitor charged and discharged current.The LCL filter are used for control the currentwhich removes the LCL resonance and maintain the stability.The results show that R,RL Load, and different modulation indeces and also grid connected load using LCL filterwhen reference current drops to 80% of full load current and also full load.

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