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Design of Fault Tolerant Array Multiplier Using Parity Preserving Reversible Gate

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Abstract:
The digital designs with Reversible logic are more popular now days because of the increased demand of low power usage. Some of the Reversible logic gates are discussed in this paper. This paper also introduces a Parity Preserving Reversible Gate (PPRG) which is used in the fault tolerant devices design such as adders, subtractors and multipliers. The design of an array multiplier by using fault tolerant parallel adders is discussed in this paper. The fault tolerant parallel adders are designed using fault tolerant full adders and half adders and these adders are designed through Parity Preserving Reversible Gate. These adders and multipliers are useful in designing complex circuits such as ALU.

Keywords: Fault Tolerant, Array Multiplier Parity Preserving, Reversible logic, Low power

1. Introduction

Low power designs with higher speed are the current trend in VLSI market. But the loss of information and the fault detection consumes much more power. When Landauer says that data misfortune attribute able to irreversibility capability contributes to energy dissemination, reversible reasoning was first associated with energy. Bennett also confirms that the only way to reach zero energy dissipation is for the circuit to have dual gates. The knowledge loss or information loss results in some extreme cases where the information vector cannot be separated from the output vector. This mainly occurs in irreversible logic gates such as NAND, NOR, OR, NOT gates etc. This information loss results in energy dissipation in the form of heat [1]. The Landauer principle states that “At least KTln2 joules ofenergy are required to delete any piece of memory.” The Boltzmann constant is K, and the absolute temperature at which the process is carried out is T. The Moore’s law states that “Processing capacity doubles every 18 months.” If this is followed, by 2020, a large amount of power loss occurs. In 1970s, Bennett and Feynman recognized this problem. In 1973, Bennett demonstrated that using of reversible logic in VLSI circuits could solve the energy dissipation problem. Zero energy dissipation is possible in reversible logic gates. In Reversible logic gates, the retrieval of information is possible as one output is considered as garbage output and it contains one input value as output. So it reduces energy consumption due to heat dissipation. This concept may become an advantage in future VLSI circuit designs. The research in this is in the works. The recently suggested complete sum multiplier [2-12] was reversible circuits for various applications. In these reversible designs, the Multiplier circuits are most important as they are the key circuits in designing of computer systems such as ALU and mobile phones such as image and sound processing applications.

1.1 Reversible and Irreversible Logic Gates

The Moore's law is at an end as perthe opinion of many researches as the reduction of transistor size is almost at an end. But the power requirements of recent technologies are more. IF power consumption is reduced, it reduces the speed. If speed is increased, it increases the power consumption. So, a compromise should be made between power consumption and speed.

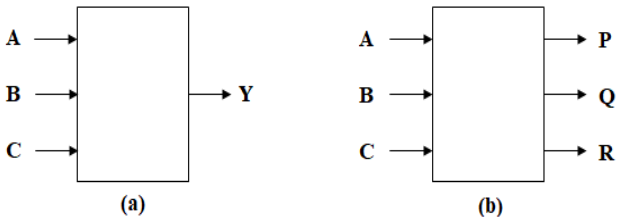

Figure 1 (a) Irreversible Logic Gate (b) Reversible Logic Gate

In irreversible logic gates the no. of inputs is not equal to the no. of outputs as shown in above figure 1(a). Due to this retrieval of data is more difficult and results in heat dissipation. This heat dissipation consumes more power. In reversible logic gates the inputs number is same as the outputs number and one of the outputs is similar to any of the input. Due to this zero energy dissipation is possible and the designs are fault tolerant. Some of the reversible gates used for reversible logic synthesis [13] are Feynman Gate, Fredkin gate, toffoli gate, Not Gate, Peres gate etc.

2. Proposed Design

Using the parity preservative reversible gate, half adder, full adder, parallel adder and multiplier [10] are designed. In this paper 2X3 and 3X2 array multipliers are discussed. By using these MXN multiplier can be designed.

2.1 PPRG

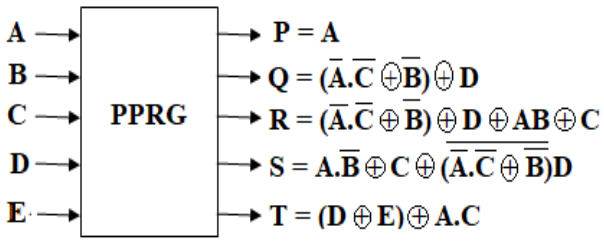

Figure 2 Parity Preservative Reversible Gate

The PPRG has A, B, C, D, E as inputs and P, Q, R, S, T as outputs. Figure 3 shows a 5*5 parity preservative reversible gate The gate acts as NOR gate at output Q when input B=1 and D=0 (Q = (A+C)'). In this gate the input parity is equal to the output parity.

2.2 PPRG Half Adder

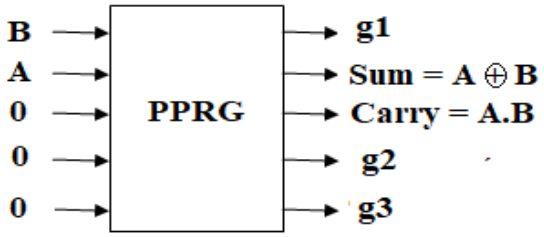

Figure 3 PPRG Half Adder

A PPRG is used as half adder to add two bits A, B and provides outputs S and Co as shown in figure 3. The inputs are applied at A & B ports of PPRG and C, D, E are equal to 0. The outputs P, S & T are garbage outputs and Q is Sum Output and R is Carry Output. The garbage outputs are labeled as g1, g2, g3. The logical expressions of half adder are

Sum = A xor B

Carry = (A and B)

2.3 PPRG Full Adder

A PPRG is used as full adderto add three bits A, B & Cin and provides outputs S and Co as shown in figure 4. The inputs are applied at A, B & D ports of PPRG and C, E are equal to 0. The outputs P, S & T are garbage outputs and Q is Sum Output and R is Carry Output. The garbage outputs are labeled as g1, g2, g3. The logical expressions of full adder are

Sum = (A xor B xor Cin)

Carry = (((A xor B) and Cin) xor AB)

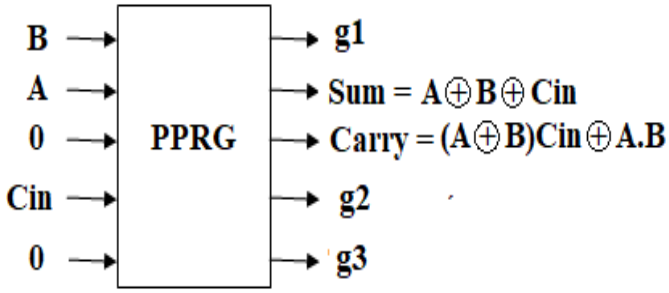

Figure 4 PPRG Full Adder

2.4 4-bit Parallel Adder

The 4-bit parallel adder adds 4-bit A (A3A2A1A0) & B (B3B2B1B0). This design requires 3 PPRG full adders and 1 PPRG half adder. In the same way, an n-bit parallel adder requires (n-1) PPRG full adders and 1 PPRG half adder. So, the same design is utilized to design an n-bit parallel adder in the design of multiplier. The figure 5 shows a 4-bit PPRG parallel adder.

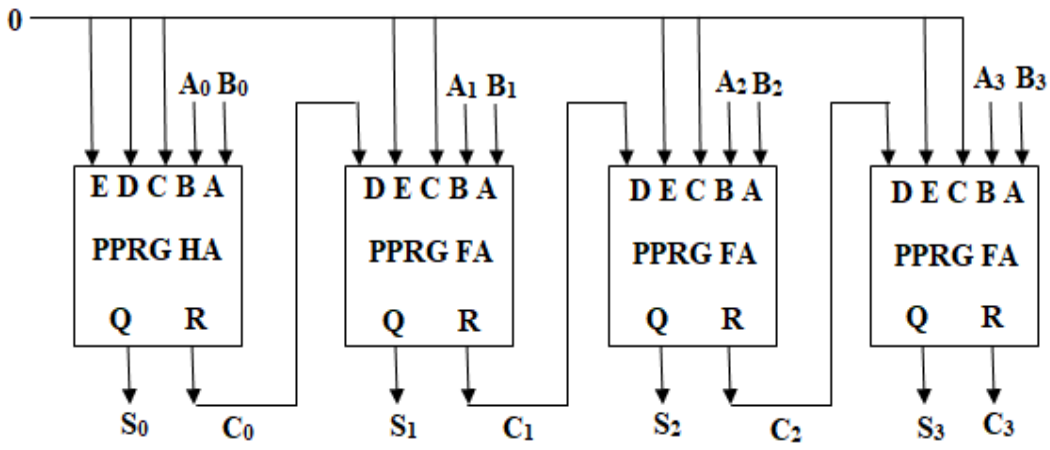

Figure 5 4-bit Parallel Adder

2.5 Array Multiplier

An array multiplier multiplies two numbers by using parallel adder. In this paper 2X3 and 3X2 multiplier designs using 4-bit PPRG parallel adder are discussed. These multipliers are low power and low heat dissipating multipliers and are useful in the audio and video processing applications.

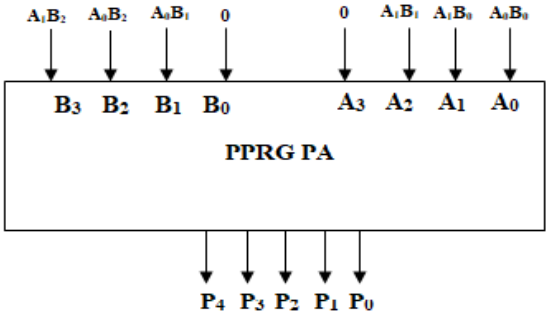

Figure 6 2X3 Multiplier

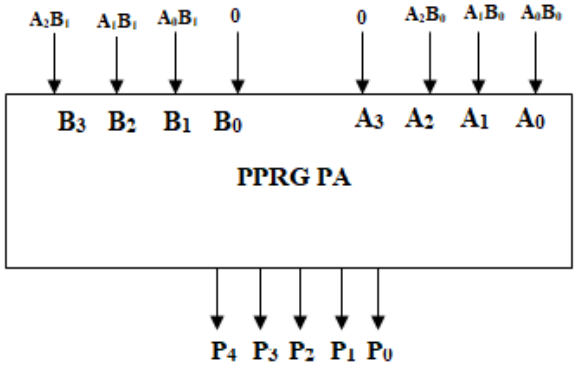

Figure 6 3X2 Multiplier

Results:

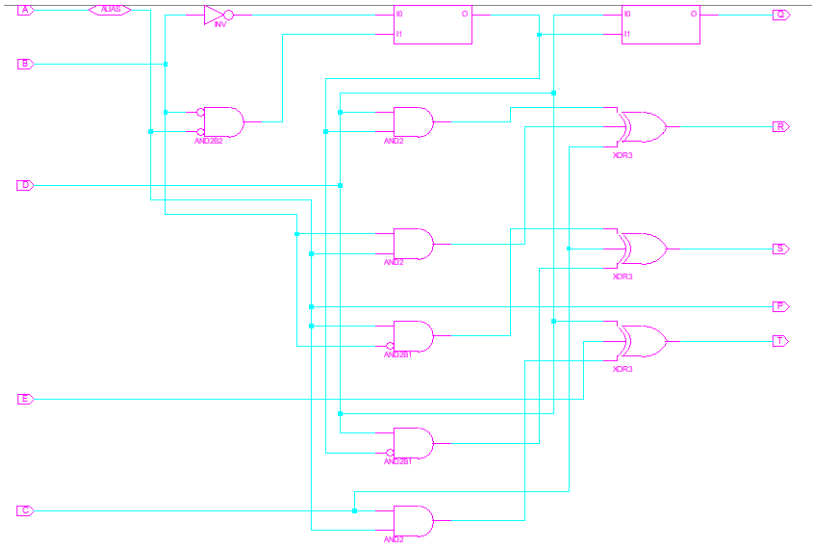

Figure 7 PPRG gate

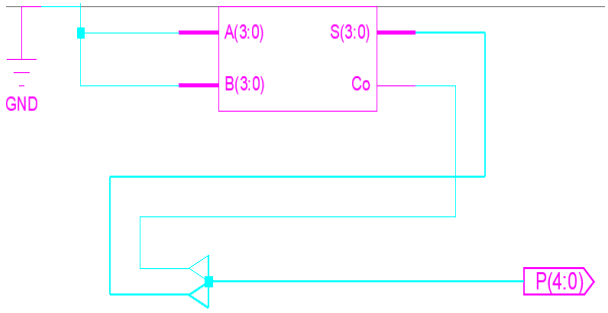

Figure 8 2X3 Multiplier using PPRG

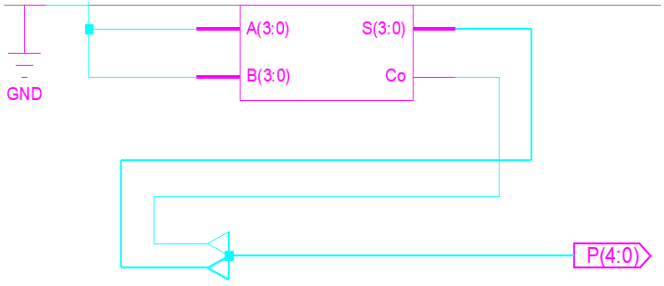

Figure 9 3X2 Multiplier using PPRG

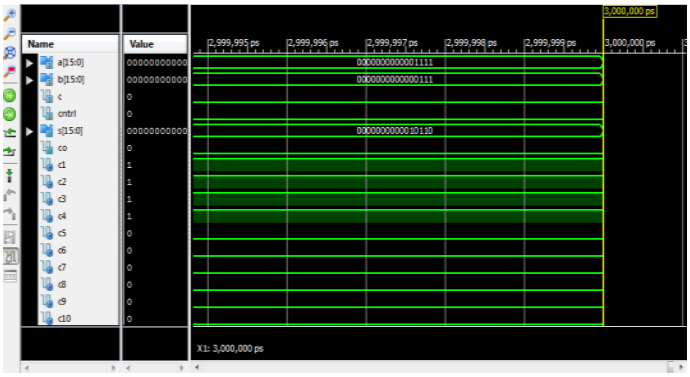

Figure 10 Simulation Results

Table 1 Comparison table of different multipliers

Component / Design	3X2 Multiplier	2X3 Multiplier
Delay	0ns	0ns
Total Memory Usage	4479872 kb	4479040 kb
Garbage outputs	12	12

3.Conclusion

The generator is a central algebraic complex number. The projected energy consumption is closely connected to their versibility of numbers we built are versible supplier with a program and Verilog in the proposed work, which has a lower door count and waste output.The table of comparisons provides a good view of thecurrentscheme.Minimizecircuitcomplexitywithreduced gate numbers. The scope for further research is on reversing complex circuits such as the function evaluation and the use of this multiplier for different divisional circuits.

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