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TCAD RF Performance Investigation of V-Shaped Groove Gate MOSFET

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Abstract
For the first time, the RF performance analysis of a V-shaped grooved (V-GG) Gate MOSFET has been presented and compared with the trapezoidal groove gate (TGG) and rectangular groove gate (RGG) MOSFETs, using ATLAS-3D device simulator, for future wireless and ULSI applications. The study reveals that V-GG MOSFET exhibits significantly enhanced performance as compared to its conventional counterparts in terms of the figure of merits (FOM): drain current, transconductance (gm), cut-off frequency (ft), maximum transducer power gain, stern stability factor (K), and, S-parameters.

Keywords: MOSFET, V-shaped grooved gate, RF applications

1. Introduction

Over the past 40 years, conventional MOSFETs have demonstrated a continuous pace of performance improvement due to aggressive device scaling at the cost of more and more complex process engineering. One of the objectives of pushing technology forward is to continue to develop opportunities for future high-speed and RF '[1-5]' applications, thus offering even greater energy efficiency for mobile devices. To pursue CMOS scaling, many challenges must be solved, such as the control of leakage currents, short channel effects (SCEs), hot carrier effects (HCEs), and parasitic capacitances which degrade the device performance.

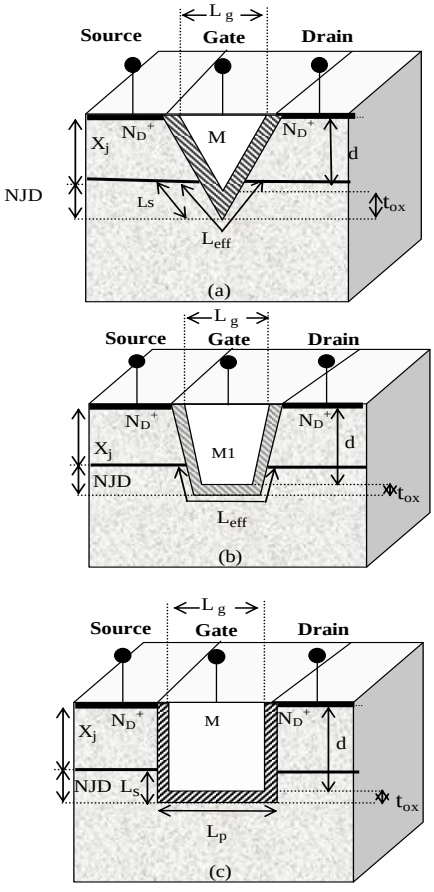
The present work concentrates on the RF performance assessment of different grooved gate structures, i.e. V-GG, TGG, and RGG MOSFETs by using the device simulator: ATLAS '[6]'. The Grooved Gate '[7, 8]' structures are considered potential candidates to suppress and overcome SCEs, punch-through, and DIBL effects even at gate lengths down to sub-100 nm regime because the negative junctions can be fabricated without any increase in the series resistance and hence, for use in CMOS ULSI circuits. This is because the grooved gate MOSFETs carry a concave device structure in which potential barriers are formed at the corners due to the high density of electric field lines, resulting in improvement of SCEs in terms of reduced punch through and drain-induced barrier lowering (DIBL) effect. However, these barriers act as a hurdle in the path of carriers, because carriers now require more

energy to surmount the barriers, which limits its carrier transport efficiency and hence, the current driving capabilities of the device. In the case of trapezoidal grooved gate (TGG) MOSFET, the height of corner barriers is comparatively low as compared to rectangular groove gate (RGG) MOSFET, which results in improved device speed and also SCEs suppression '[8]'. Furthermore, in V-GG there is only one potential barrier exists. The structure thus provides an easier path for carriers as compared to its conventional counterparts. This results in improved RF performance due to reduced SCEs and HCEs; and improved carrier transport efficiency, thereby proving its efficacy for high-performance wireless and ULSI applications.

2. Result And Discussion

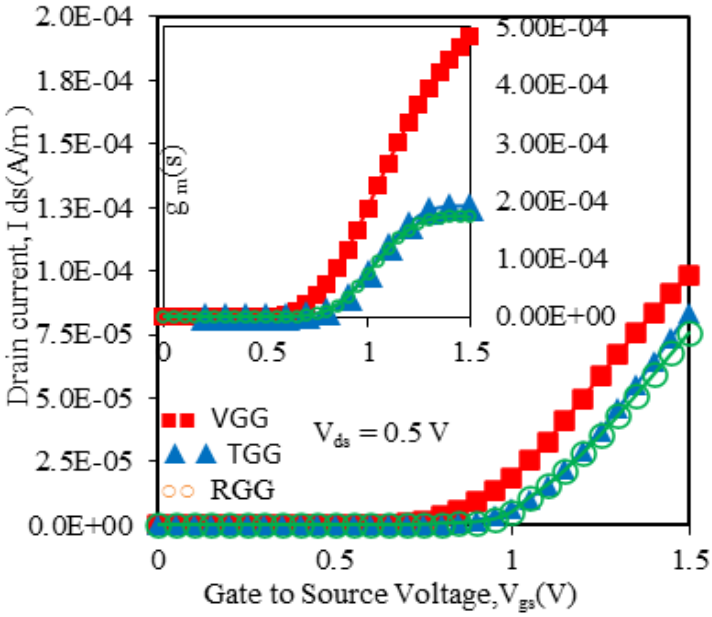
A schematic cross-sectional view of different recessed channel structures considered in this study i.e., V-GG, TGG, and RGG MOSFETs are shown in "Fig. 1(a-c)" respectively. The effective channel length L_{eff} corresponds here to the metallurgical channel length, taken along the gate oxide. For TGG and RGG MOSFET, Leff = (2Ls) + Lp. where Lp is the planar part and Ls is the angular part of the channel. While for V-GG Leff = 2Ls. "Fig.1a" Schematic structure of V-GG MOSFET having gate length (Lg)=50nm, Groove Depth (d)=76nm, NA =1x10^{17} cm^{-3}, ND=1x10^{20} cm^{-3}, W=1µm, t_{ox}=4nm. Work function Φ_M=4.77eV. "Fig. 1b" Schematic structure of TGG MOSFET having gate length (Lg)=50nm, Groove Depth (d)=76nm, NA =1x10^{17} cm^{-3}, ND=1x10^{20} cm^{-3}, W=1µm, t_{ox}=4nm. Work function ΦM=4.77eV. "Fig. 1c" Schematic structure of RGG MOSFET having gate length (Lg)=50nm, Groove Depth (d)=76nm, NA =1x10^{17} cm^{-3}, ND=1x10^{20} cm-3, W=1µm, tox=4nm. Work function ΦM=4.77eV.

Figure 1: Schematic view of V-GG, TGG, and RGG MOSFETs



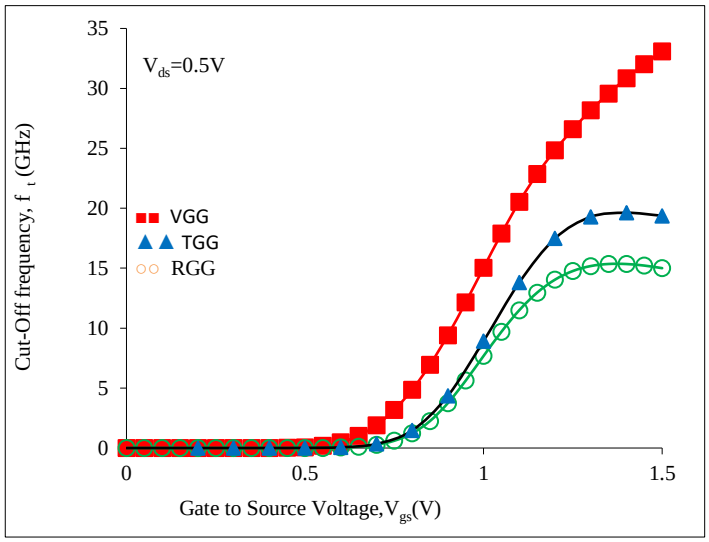
"Fig. 2" shows the drain current variation and (inset) shows the transconductance variation of V-GG, TGG, and RGG MOSFETs with gate bias voltage. It is true that the recessed channel MOSFETs reduce the SCEs and HCEs of the device which are more prominent as we go down to the sub-100 nm regime. This happens due to the presence of negative junction depth (NJD) which prevents the impact of potential variations at the drain side. However, on the same side due to these NJDs, potential barrier appears at the corners as a consequence of the high density of electric field lines [7]. These barriers serve as an obstacle in the path of the carriers which reduces the carrier transport efficiency of the device. In TGG MOSFET, the height of these barriers is lower as compared to RGG MOSFET. This results in enhanced carrier transport efficiency which in turn increases the drain current and transconductance in TGG MOSFET, as shown in "Fig. 2" and (inset), respectively. Furthermore, in V-GG, there is only one obstacle present in the path of carrier transport. This serves as an advantage in reducing SCEs and improving carrier transport efficiency which leads to enhanced drain current and transconductance, as shown in "Fig. 2" and it's (inset).

Figure 2: and it's (Inset) show a variation of drain current and transconductance, respectively with gate bias for V-GG, TGG, and RGG MOSFETs.



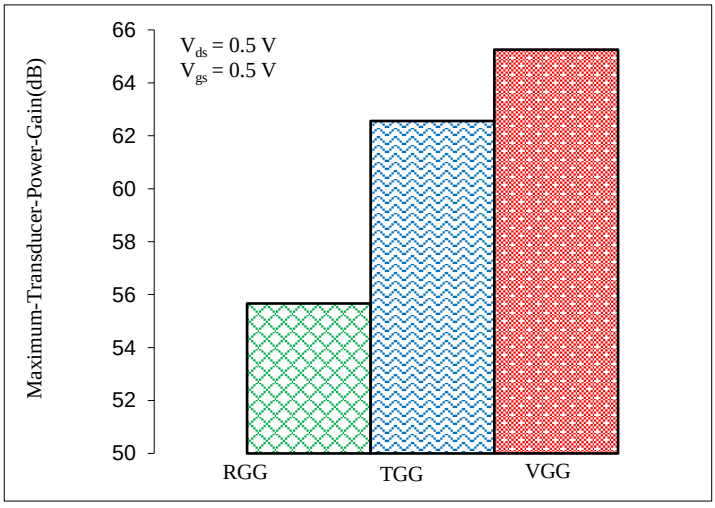
An important parameter for RF performance evaluation is the cut-off frequency (ft) which is defined as the frequency for which the magnitude of the short circuit current gain drops to unity. "Fig. 3" shows the cut-off frequency variation for V-GG, TGG, and RGG MOSFETs with gate bias. The figure clearly shows that V-GG exhibits the largest ft as compared to its conventional counterparts as a consequence of the enhanced transconductance and drain current, owing to the presence of a single corner potential barrier as discussed earlier. An important parameter for RF performance evaluation is the cut-off frequency (ft) which is defined as the frequency for which the magnitude of the short circuit current gain drops to unity. Fig. 3 shows the cut-off frequency variation for V-GG, TGG, and RGG MOSFETs with gate bias. The figure clearly shows that V-GG exhibits the largest ft as compared to its conventional counterparts as a consequence of the enhanced transconductance and drain current, owing to the presence of a single corner potential barrier as discussed earlier.

Figure 3: Variation of the cut-off frequency with gate bias for V-GG, TGG and RGG MOSFETs.



Moreover, maximum transducer power gain (GMT) is the most meaningful description of power transfer capabilities for an amplifier design as it compares the power delivered to the load with the power that the source is capable of supplying under optimum conditions. Also, the high-frequency performance of a device is typically done by using unilateral power gain. “Fig. 4” shows GMT at frequency 1x107Hz and “Fig. 5” shows the frequency variation of unilateral power gain for V-GG, TGG, and RGG MOSFETs. It is seen that as we move towards a more prominent device, i.e. from RGG to TGG and then to V-GG MOSFET, there is a considerable enhancement in the power gains. This improvement is basically due to the enhanced carrier transport efficiency, gate control, and cut-off frequency of the device thereby proving its efficacy for future wireless and RF applications. Furthermore, in the presence of feedback paths from the output to the input, the circuit might become unstable for certain combinations of source and load impedances. A Low Noise Amplifier (LNA) design that is normally stable might oscillate at the extremes of the manufacturing or voltage variations, and perhaps at unexpectedly high or low frequencies.

Figure 4: Maximum transducer power gain (GMT) at 1x10^7Hz frequency V-GG, TGG, and RGG MOSFETs.



The Stern stability factor characterizes circuit stability as in the equation below:

$$K = \frac{1+|\Delta|^2 - |S_{11}|^2 - |S_{22}|^2}{2.|S_{12}.S_{21}|}$$

where, S_{11} and S_{22} are the reflection coefficients and S_{12} and S_{21} are the transmission coefficients shown in Fig. 9 and s-matrix △ is defined as:

$$\Delta = S_{11}.S_{22} - S_{12}.S_{21}$$

Figure 5: Variation of unilateral power gain with frequency for V-GG, TGG, and RGG MOSFETs

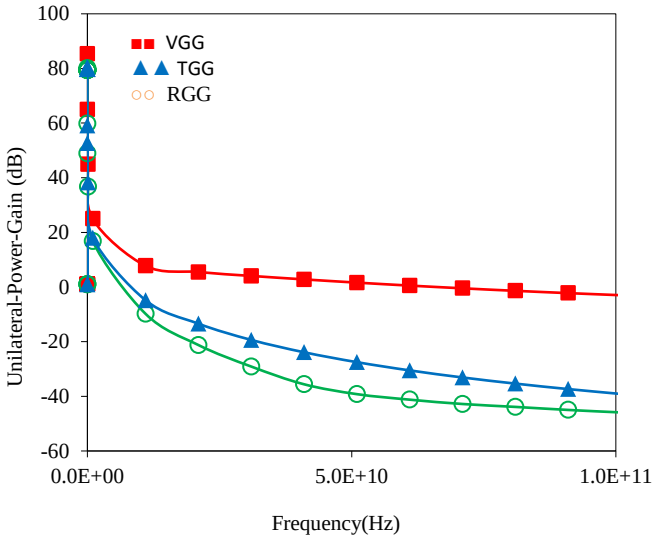
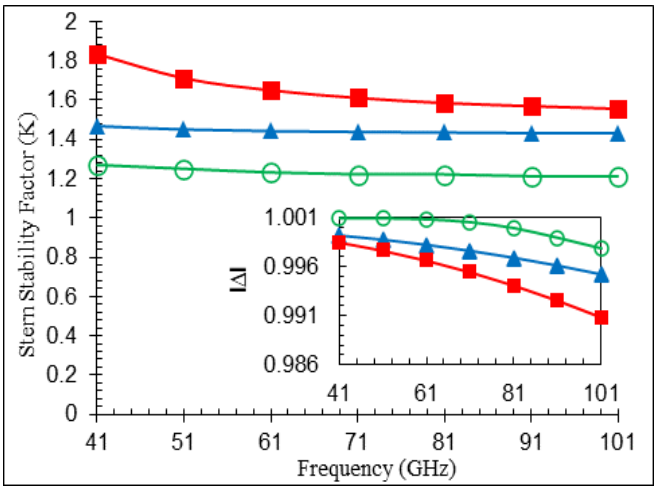


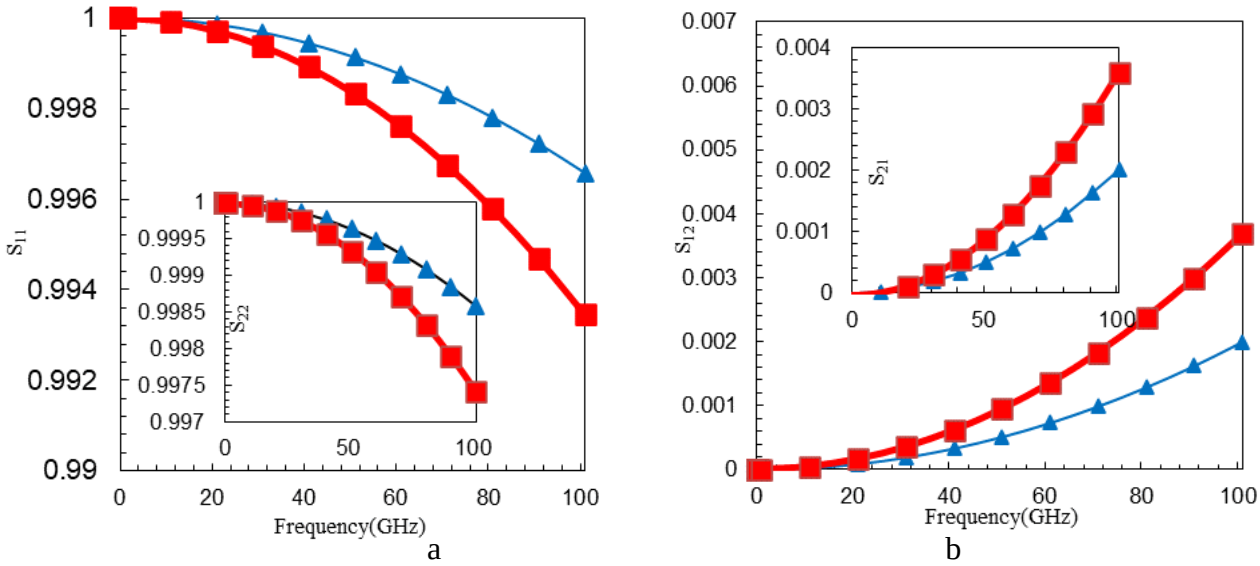
Figure 6: Variation of Stern stability factor at a higher frequency.
(Inset) Variation of △ at higher frequency for V-GG, TGG, and RGG MOSFETs.



"Fig. 6" and its 'inset' show the variation of K and △, respectively, at higher frequencies. When K >1 and △<1, the circuit becomes unconditionally stable i.e. independent of source and load impedances; thereby maximizing the power transfer. As is clear from the figure, K is appreciably increasing and △ is decreasing as the frequency increases, for V-GG MOSFET in comparison to TGG and RGG MOSFETs; reflecting the less oscillatory nature of V-GG MOSFET even at high frequencies. Moreover, "Fig.

7(a,b)" proves the superior characteristics in terms of S_{11} and S_{22}, reflection coefficients, and S_{12} and S_{21}, transmission coefficients for V-GG over TGG MOSFET, owing to the better device performance of the newly proposed design. Hence, V-GG design is proved to be superior to its conventional MOSFETs thus, proving as a potential candidate for high-speed logic.

Figure 7(a,b): show the variation of the reflection coefficient, i.e. S_{11} and S_{22}, and transmission coefficient, i.e. S_{12} and S_{21}, at a higher frequency for V-GG and TGG MOSFETs.



3. Conclusion

In this work, the RF performance investigation of V-GG MOSFET has been carried out for the first time and compared with conventional TGG and RGG MOSFETs by using a device simulator: ATLAS bringing out its potential as an excellent candidate for wireless and RF applications. Results clearly depict that, V-GG MOSFET exhibits superior performance as compared to RGG and TGG MOSFET in terms of improved carrier transport efficiency and hence, the transconductance and reduced parasitic capacitances, which further contribute towards the improvement in cut-off frequency. Further, for optimizing the performance and reliability of nanoscale V-GG MOSFET for high-speed logic and RF applications, maximum transducer power gain (GMT), maximum unilateral power gain (MUG), stern stability factor (K) S-parameters are evaluated and compared with conventional counterparts. Results reveal that, due to improved gate controllability, driving current, and reduced parasitic capacitances, V-GG MOSFET shows great potential for high-performance, RF/Microwave application.

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