International Journal for Multidisciplinary Research (IJFMR)
E-ISSN: 2582-2160 ● Website: www.ijfmr.com ● Email: editor@ijfmr.com

# Design and Implementation of High-Performance Power-Efficient Multiple-Output Class-AB Current Mirror for Capacitance Multiplier and Precision Rectifiers

**Sonam Pal A[1], Dr. J.C Narayana Swamy[2]**

[1]VLSI Design and Embedded System, Bangalore Institute of Technology, Bengaluru, India
[2]Associate Professor, Department of ECE, Bangalore Institute of Technology, Bengaluru, India

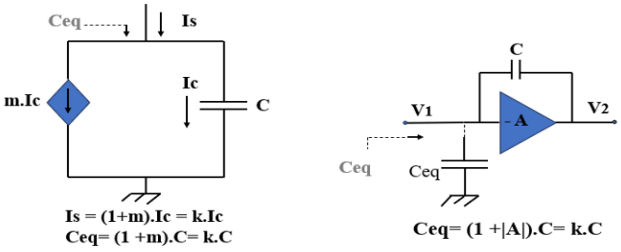
**Abstract**
The development of high-efficiency capacitance multipliers and precision rectifiers for VLSI (Very Large-Scale Integration) systems is examined in this work, with a focus on low voltage operation. The major goal is to reduce supply voltage in order to consume energy as little as possible. It has been successfully created for the capacitance multiplier to work properly even with extremely low voltage supply, as low as 0.25 V. Class-AB current mirrors, which are renowned for their outstanding current efficiency, are used in the design. Experimental measurements were made on a 180-nm CMOS-based capacitance multiplier that obtained a multiplication factor of 11 in order to assess performance. The same class-AB current mirrors were also used in the same CMOS technology to construct low-voltage precision rectifiers. Over a hundred times more output current than quiescent current is produced by these rectifiers. Notably, both circuits function with 0.25 V supply and dissipate static power at a rate of only 100 nW. The work shows that low-voltage designs and class-AB current mirrors can be used to produce great performance and efficient power usage in VLSI systems.

**Keyword:** Class-AB Current Mirror, Capacitance Multiplier, Precision Rectifiers, Low Supply Voltage.

## I. INTRODUCTION

In particular, portable and biomedical devices have a rising need for VLSI systems that run on low voltage and little power. Reduced minimum supply voltage needs (Vsupplymin=(VDD-VSS) min) and low quiescent current in these systems are needed to meet this demand. Low-voltage operation is required for contemporary CMOS technologies that run on subvolt supply (VDD<1 V). Very low supply voltages are ideal for current-mode (CM) systems, in which input-output and intermediate variables are expressed as currents. Since it permits voltage-to-current conversion and serves as a bridge between external input voltage signals and the internal input current signals needed by CM systems, a low-voltage linear operational transconductance amplifier (OTA) is frequently crucial for these systems.

Capacitance multiplication (Cap-Mlts) is a method frequently employed in VLSI systems to lessen the necessary silicon area. In order to achieve an equivalent capacitance ($C_{eq}$) that is a multiple ($k$) of the base capacitance ($C$), where $C_{eq} = kC$, active devices must be used.




(a) (b)

**Fig. 1. Methods using a capacitance multiplier. (a) Current-mode. (b) Voltage-mode.**

Capacitance multiplication can be accomplished using either the CM (current mode) or VM (voltage mode) methods. A current mirror is used in capacitance multiplication (CM) to multiply the capacitor current (Ic) by m. Source current (Is) equal to (1+*m*) Ic is produced when the output of the current mirror is linked to the signal terminal driving the capacitor. With $k = 1+m$, this design results in an equivalent capacitance.

$$C_{eq} = (1+m)\, C = kC \qquad (1)$$

Whereas the Voltage Multiplier (VM) method of capacitance multiplication, shown in Figure 1.1(b), depends on the Miller effect and requires the use of an active element as a multiplier. Usually, this active component is an inverting amplifier with a gain of |*A*|. As a result, the formula $k = 1+|A|$ is used to calculate the effective capacitance.

$$C_{eq} = (1+|A|)\, C = kC \qquad (2)$$

Due to their simplicity and ability to function with low supply voltages, CM capacitance multipliers based on current mirrors are favoured over VM capacitance multipliers. In feedforward circuits with low impedance nodes in the signal line, they also provide high speed performance. In contrast, because of the saturation of the amplifier's output node, VM circuits consume more power and have a smaller dynamic range. Additionally, when the gain (*A*) increases in VM circuits, the bandwidth of the amplifiers drops, resulting in a smaller frequency range for capacitance multiplication. It is important to keep in mind that the maximum output current of CM capacitance multipliers is constrained by the output branch's bias current. This restriction has an effect on the slew rate, dynamic range, and the highest value of k that may be obtained. When employing sine-wave voltage signals with a maximum amplitude ($A_p$) and frequency (*f*), the maximum current ($I_{cMAX}$) delivered to Ceq is provided by

$$I_{cMAX} = 2\pi f A_p kC = 2\pi f A_p C_{eq}. \qquad (3)$$

Limitations on parameters like $A_p$, *f*, or *k* can be circumvented by increasing the bias current in the $I_{cMAX}$ circuit. The overall power consumption and static power dissipation will rise as a result, though. When compared to the bias current, Class-AB circuits have a greater peak input-output current, which is influenced by their current efficiency (*CE*). The ratio of the total supply quiescent current ($I_{supplyQ}$) to the maximum output current signal ($I_{outMAX}$) represents the current efficiency.

$$CE = I_{outMAX} / I_{supplyQ} \qquad (4)$$

There are certain issues with using self-biased current reflectors to implement class-AB CM capacitance multipliers. The necessity for a sizable supply, poorly controlled quiescent current, and the potential loss in output resistance and copying accuracy are some of these downsides. While maintaining a low quiescent power dissipation, a high current efficiency enables the achievement of a higher capacitance multiplication factor. In many applications, precision rectifiers are crucial for converting AC signals to

DC. Operational amplifiers have been widely employed, however their bandwidth and speed are constrained. Although cascoding current mirrors can increase precision and linearity at the expense of greater supply requirements and constrained output currents, it can increase bandwidth and speed. To overcome these difficulties, the research suggests a high-performance class-AB current mirror-based low-voltage CM capacitance multiplier. With this method, low-voltage operation is possible, precision and linearity are improved, and strong common-mode rejection is offered. The efficiency of the method for enhancing precision rectifier performance is demonstrated in the paper, which includes technical details and experimental validation.

## II. REVIEW OF PREVIOUS WORKS

A high-performance capacitance multiplier using adaptively biased class-AB current mirrors was used to amplify effective capacitance at low supply voltages in order to decrease power consumption in VLSI systems [1]. Experimental measurements conducted on a fabricated prototype validated its effectiveness by demonstrating an impressive 11-fold increase in capacitance. The same current mirrors were also used to create low-voltage precision rectifiers with output currents that were more than 100 times greater than the quiescent current. Surprisingly, both circuits demonstrated static power dissipation of only 300 nW when run with 0.25 V supply, greatly assisting in the reduction of overall power in VLSI systems. The paper presents a novel technique for improving CMOS differential amplifier circuits by enhancing linearity and expanding the differential input voltage range. The approach involves a unique current biasing method that combines constant current with a current proportional to the square of differential input voltage. This technique effectively reduces circuit distortions and improves the bandwidth of the differential structure [2]. The circuit has a minimum supply voltage of 1.5V and a maximum differential input voltage range of about 200mV, making it specifically intended for low-voltage and low-power tasks. To verify the theoretical projections, SPICE simulations are run, highlighting the good performance of the suggested differential circuit. The research centers around utilizing a Voltage Differencing To build a capacitance multiplier circuit, use the Transconductance Amplifier (VDTA)[3]. By translating the voltage difference across the input capacitance into a current and amplifying it, the capacitance multiplier increases the effective capacitance without physically adding larger capacitors. The proposed design achieves a multiplication factor of 115. This approach saves space on integrated circuits, which is advantageous in designs with area constraints. The researchers validated the design through simulations using the Cadence software and specifically evaluated it using the 0.18μm TSMC technology, gaining insights into its feasibility and performance before fabrication. Simulations help analyze the circuit's functionality, performance, and behavior, identifying potential issues or areas for improvement before actual fabrication. [4]. This study focuses on the implementation of a large input dynamic range, linearly controllable transconductance, CMOS voltage differencing transconductance amplifier (VDTA). In order to accomplish linear tuning of the transconductance, the long-tail bias current is squared in the suggested design method. Source degradation is also used to increase linearity. The use of this linearly tunable VDTA in an electrically programmable all-pass filter circuit serves as proof of its efficacy. PSPICE software was used to simulate the suggested circuit and its use with TSMC 0.25-m CMOS technology. This paper introduces a novel capacitance multiplier design utilizing Second Generation Current Conveyors (CCIIs) [5]. CCIIs are ideal for incorporation into integrated circuits because they have desirable properties including high bandwidth and low power consumption. The paper focuses on discussing CCII non-idealities and how they affect capacitance multiplier design. By comparing the

outcomes with theoretical predictions, SPICE simulations are carried out to validate the design and evaluate its practical applicability. The suggested design's dependability and efficacy are guaranteed by this verification method. An efficient CMOS Fully Differential Difference Amplifier (FDDA) design for low-voltage and low-power applications is presented in this brief [6]. The design incorporates a single differential pair with multiple-input bulk-driven MOS transistors (MI-BD MOSTs), resulting in reduced power consumption. Despite operating at 0.5 V and consuming only 246.6 nW, the circuit offers desirable features such as rail-to-rail input common mode range, high common-mode rejection ratio (CMRR) and power supply rejection ratio (PSRR), voltage gain, gain bandwidth product, and low total harmonic distortion (THD). The design and simulation were performed using the Cadence/Spectre environment with a 0.18 µm CMOS process from TSMC.

## III. PROPOSED METHODOLOGY

Through the use of quasi-floating gate (QFG) approaches, the constraints of the conventional class-A current mirror are addressed in Figure 2. These methods make use of massive RC networks made up of the capacitors C1, C2, and C3, as well as high-value resistances RQFG that are implemented as pseudo resistors utilising small transistors. The input current (Iinp) determines the cascode voltages (Vbp, Vcp, and Vcn), which can be dynamically adjusted using QFG techniques. The resistances RQFG are incredibly huge, measuring somewhere around 10 gigohms, while the capacitors C1, C2, and C3 have comparatively tiny values in the picofarad region. High-pass circuits with a typical 3-dB cutoff frequency in the low hertz region are produced using this arrangement. Although differences in the manufacturing process and temperature of C1, C2, C3, and RQFG may cause the actual value of the adjusted f3-dB to vary slightly, these fluctuations do not significantly affect the performance of the class-AB circuit. These variances are not a serious issue as long as the modified f3-dB stays below the lowest frequency present in the processed signal.

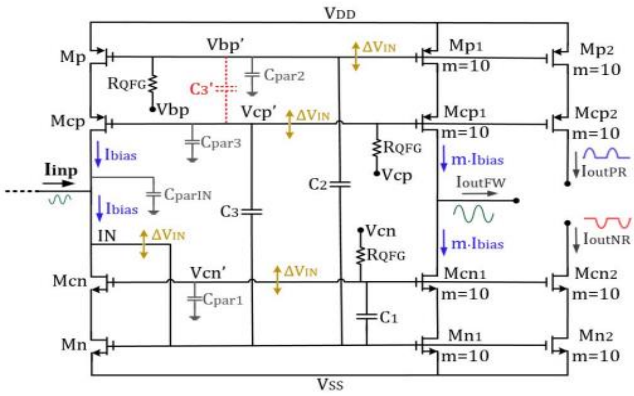



**Fig. 2. Block diagram of power-efficient class-AB current mirror with multiple outputs**

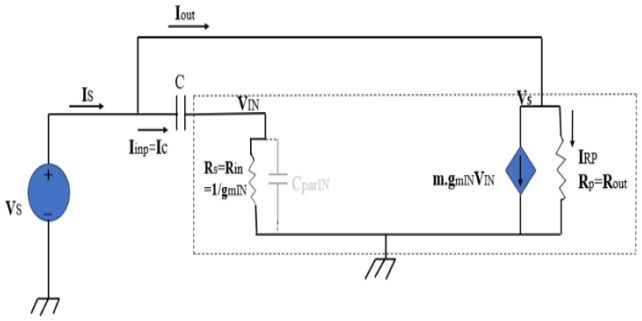
The voltages at nodes V'bp, V'cp, and V'cn are identical to Vbp, Vcp, and Vcn, respectively, under static conditions. Transistors of multiplicity m have a quiescent current of m Ibias, while transistors of PMOS and NMOS have equal currents of Ibias. The capacitors C1, C2, and C3 function as floating batteries during dynamic operation, converting changes in VIN (produced by Iinp) to the voltages Vcn, Vbp, and Vcp. NMOS transistors handle positive input currents, and PMOS transistors handle negative input currents. The voltage at node IN rises in response to positive input current signals, and is subsequently sent to the nodes Vcn, Vbp, and Vcp via the capacitors C1, C2, and C3. As a result, the NMOS transistors'

current increases while the PMOS transistors' current decreases. This gives the NMOS mirroring transistors greater headroom for their drain-source voltage, enabling them to handle bigger currents. These currents can have peak values that are far higher than bias currents since they are not constrained by the quiescent current. As a result, the circuit operates in class-AB with high current efficiency (CE). Without the voltage headroom (VSGp) of a diode-connected PMOS transistor on the input branch for supply requirements, the PMOS component of the circuit performs as a PMOS mirror. This is because transistor Mp behaves as a diode-connected transistor for signals because nodes IN and Vbp are AC coupled by C2. In order to prevent voltage dividers created by C2 and C3 with the parasitic capacitances Cpar2 (at node Vbp) and Cpar3 (at node Vcp), C3 is substituted with C3 to enable smaller values of C1, C2, and C3. Compared to other class-AB mirrors, the class-AB current mirror has better linearity, reduced supply requirements, a larger output current range, and a higher power efficiency. It is appropriate for a variety of CM applications, including precision rectifiers and CM capacitance multipliers. By connecting numerous output stages with binarily weighted scaling gain factors by switches, the class-AB mirror can also be quickly converted into a gain-programmable mirror, enabling digitally changeable factor m.

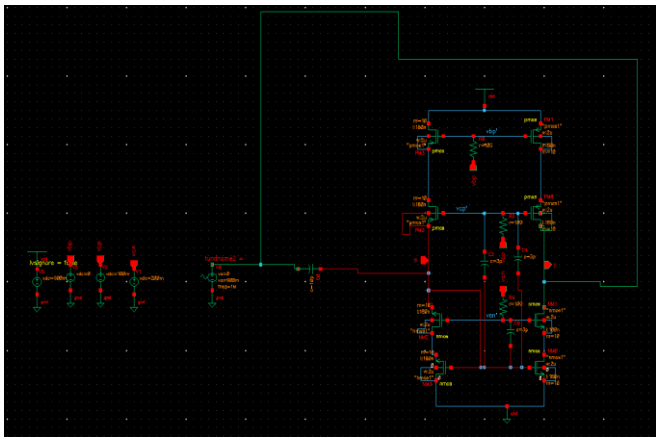
A. Class AB Capacitance Multiplier

The application of the class-AB mirror, which permits a capacitance multiplication factor of $k = (1 + m)$, is shown in Figure 3. As we have previously mentioned, the current mirror's output branch functions as a current source with an m-dependent gain. The source current, Is, is made up of the output current, Iout = $m$ * Ic * Is = (1 + m) * Ic, and the capacitance current, Ic = Iinp.

It is crucial to take into account the non-ideal effects of the input resistance (Rin) of the mirror at node IN, which is in series with the capacitor C, while putting this circuit into practice. The mirror's output resistance (Rout), which is linked in parallel with Vs, should also be considered. The frequency range over which the circuit exhibits high Q behavior as a capacitor is affected by these resistances, which are referred to as equivalent series resistance (Rs) and parallel load resistance (Rp), respectively.




(a)



(b)

**Fig. 3. (a) Block Diagram of Class-AB Capacitance Multiplier with Multiplication Factor. (b) Transistor-Level Implementation of Class-AB Capacitance Multiplier.**

Transconductances of transistors Mn and Mp, designated as gmn and gmp, respectively, have an impact on resistance Rs. Transistor Mp performs as a 1/gmp-resistance, diode-connected transistor in the AC domain. As a result, the combination of these two transistors determines the overall resistance Rs.

$$R_s = R_{in} \approx \frac{1}{g_{mn}} \left\| \frac{1}{g_{mp}} = \frac{1}{(g_{mn}+g_{mp})} = \frac{1}{g_{mIN}} \right.$$

Resistance Rs is influenced by the transconductances of transistors Mn and Mp, denoted as gmn and gmp, respectively. In the AC domain, transistor Mp operates as a diode-connected, 1/gmp-resistance transistor. Thus, the total resistance Rs is determined by the interaction of these two transistors.

$$= \frac{R_p\left(1+s\frac{C+C_{parIN}}{g_{mIN}}\right)}{1+s\left((1+m)R_pC+\frac{C+C_{parIN}}{g_{mIN}}\right)+s^2\left(\frac{R_pCC_{parIN}}{g_{mIN}}\right)}$$

$$= \frac{R_p\left(1+\frac{s}{\omega_z}\right)}{\left(1+\frac{s}{\omega_{pd}}\right)\left(1+\frac{s}{\omega_{pnd}}\right)}$$

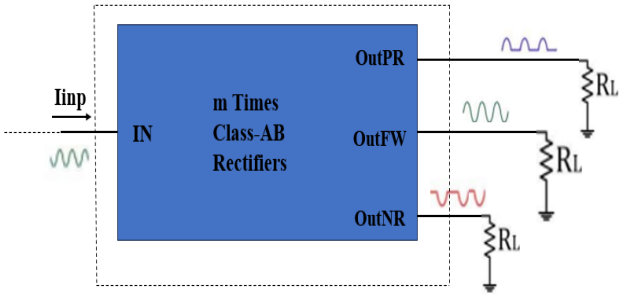
The simplified small signal model of the capacitance multiplier is shown in Figure 3, and the input impedance (Zs = Vs/Is) can be calculated using the formula below. By adding the capacitance contributions from different components, the total parasitic capacitance at node IN, denoted as CparIN, is determined. CgsMn, CgdMcn, CgdMcp, CdbMcn, and CdbMcp are among these elements.

The following is the equation for the reduction of Zs:

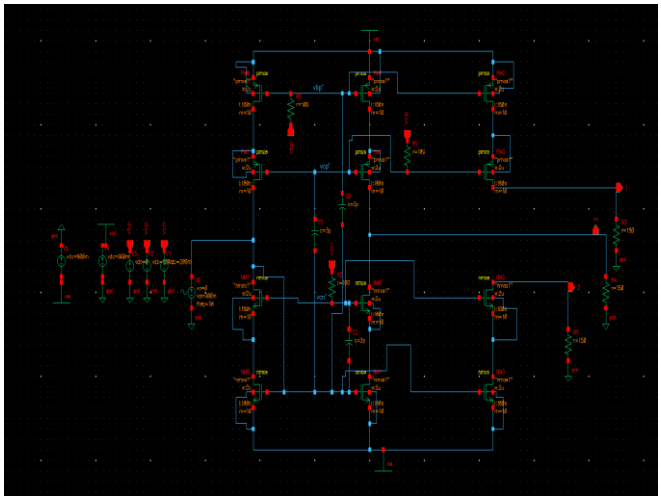
B. Class AB Precision Rectifiers

$$Z_s(s) \approx \frac{R_p\left(1+\frac{s}{\omega_z}\right)}{\left(1+\frac{s}{\omega_{pd}}\right)} = \frac{R_p\left(1+s\frac{C}{g_{mIN}}\right)}{1+s\left((1+m)R_pC+\frac{C}{g_{mIN}}\right)}$$

$$= \frac{1}{(1+m)}\left(\frac{1}{sC}+R_s\right)\left\| R_p.\right.$$




(a)

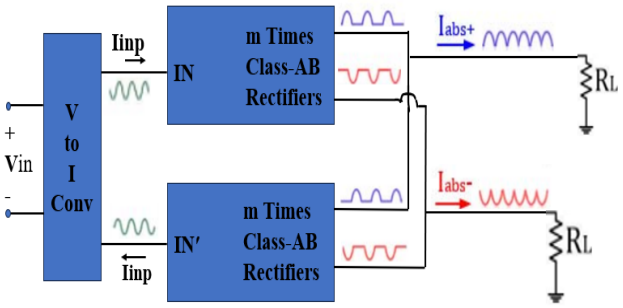


(b)

**Fig. 4. (a) Block Diagram of Class-AB Positive and Negative Half-Wave Rectifiers. (b) Transistor-Level Implementation of Class-AB Positive and Negative Half-Wave Rectifiers.**

As shown in Figure 3, the class-AB current mirror design in Figure 4 can also be used to build very common-emitter low-voltage precision rectifiers. The NMOS and PMOS transistors handle the positive and negative half cycles of the input current signal Iinp, respectively, much like the prior design. The half-wave negative and positive rectified versions of the input current signal are represented by IoutNR and IoutPR, respectively, which are produced by output branches made entirely of NMOS or PMOS transistors. In order to transform the output currents into output voltages, resistors RL (or trans resistance amplifiers) might be used, as in VOutPR = IoutPR * RL.

(a)



(b)

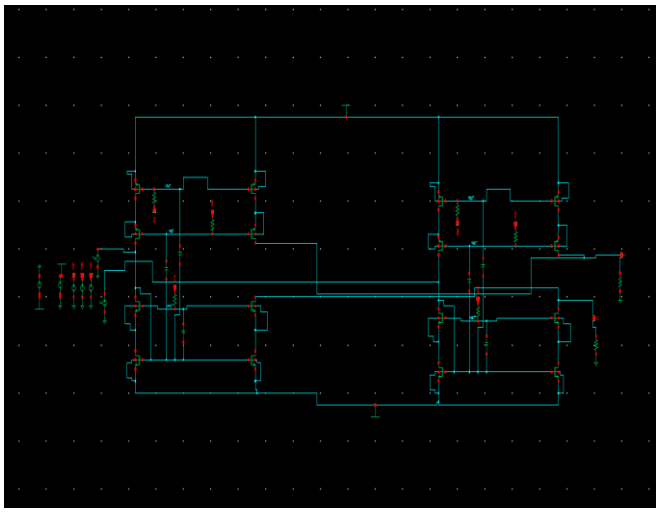


**Fig. 5. (a) Block Diagram of Class-AB Positive and Negative Full-Wave Rectifiers. (b) Transistor-Level Implementation of Class-AB Positive and Negative Full-Wave Rectifiers.**

Two half-wave corrected signals are combined during the full-wave rectification process, one of which is inverted. Two class-AB current mirrors with corresponding positive and negative half-wave rectified outputs are linked in parallel to accomplish this. Through the use of a fully differential linear voltage-to-current converter, which serves as the interface between the input voltage signal and the CM (complementary metal-oxide semiconductor) system, these current mirrors produce complementary input current signals. Other methods involve employing a different current mirror to invert one of the half-wave rectified signal components; however, this introduces delay and causes crossover distortion in the full-wave rectified output, lowering the rectifier's maximum operating frequency. The proposed full-wave rectifier in Figure 3.4, in contrast, has the benefit of simultaneously producing all half-wave signal components, ensuring that they all incur the same delay. By doing so, crossover distortion is removed and higher operating frequencies are made possible. They can be used in mobile devices, biomedical devices, communication systems, signal processing systems, and systems for collecting energy. These circuits provide numerous electronic systems and gadgets with increased efficiency, accuracy, and performance.

## IV. RESULTS AND DISCUSSION

Using 180-nm CMOS technology, the capacitance multiplier and precision rectifiers were built and simulated. The transconductance parameters in this technology are 280 A/V2 for NMOS and 50 A/V2 for PMOS transistors, with the threshold voltages for NMOS transistors being roughly 0.23 V. Unit NMOS and PMOS transistor sizes were determined to be 2/0.18 and 2/0.18, respectively. Using a method that requires using minimum-size transistors as pseudo resistors, RQFG (quasi-floating gate) is implemented. In order to reach high resistance values and properly implement RQFG in the circuit, these transistors function as resistors. Transistors with size of 0.22/0.22 were employed for the simulations. The base capacitor C was set to 10 pF, and the capacitances C1, C2, and C3 were each set to 3 pF. The 25 pF load capacitance was chosen. The bias and Ibias voltages were produced using the conventional circuitry. Two sets of supply voltages and bias currents were used during the simulation:1) VDD = 0.9 V, VSS = 0 V are the nominal dual-supply voltages. The operation was in moderate inversion, with the threshold voltage (VTH) and VGS roughly equal.2) Low dual-supply voltages: Ibias is 50 nA, VDD is 0.25 V, and VSS is

-0.25 V. The operation was in the weak inversion area, and the threshold voltage (VTH/2) was almost equivalent to VGS.

| Nominal Dual Supply Voltages $V_{DD}$=+0.9V, $V_{SS}$=-0.9V and $I_{bias}$ = 1µA | W/L (µm/µm) | $I_D$ (µA) | $V_{TH}$ (V) | $V_{GS}$ (V) | $V_{DS}$ (V) | $g_m$ (µA/V) | $g_{ds}$ (µA/V) | $g_m/I_D$ ($V^{-1}$) |
|---|---|---|---|---|---|---|---|---|
| | 2/0.18 | 1.05 | 0.238 | 0.345 | 0.169 | 25.3 | 0.232 | 24.09 |
| **Low Dual Supply Voltages $V_{DD}$=+0.25V, $V_{SS}$=-0.25V and $I_{bias}$ = 50nA** | W/L (µm/µm) | $I_D$ (nA) | $V_{TH}$ (V) | $V_{GS}$ (V) | $V_{DS}$ (V) | $g_m$ (µA/V) | $g_{ds}$ (µA/V) | $g_m/I_D$ ($V^{-1}$) |
| | 2/0.18 | 45 | 0.238 | 0.119 | 0.100 | 1.23 | 0.014 | 27.33 |

**Table 1 The proposed circuits Parameters Values**

For the proposed circuits, Table 5.1 gives simulated values for the parameters VGS, VDS, VTH, gm, and gds. It should be remembered that at nominal and low supply voltages, respectively, NMOS and PMOS transistors with the same bias current have transconductance gains, gm, of around 25 A/V and 1.2 A/V. Scaled transistors' transconductance gain, gm, grows in direct proportion to their size. Figures 5.3(a) and 5.5(a) show that at nominal supply voltages, the proposed class-AB precision rectifiers may maintain a low output quiescent current of just 12 A while achieving a dynamic output current ($I_{outMAX}$) of up to 3 mA. As seen in figures 5.3(b) and 5.5(b), the rectifiers can still produce a sizable output current of roughly 200 A at lower supply voltages while retaining a very low output quiescent current of only 0.55 A.
As the highest output current surpasses the quiescent output current in both situations, the CE is high. When the output currents at the crossover points are so small in comparison to the input current signal that the operating frequency is constrained. The highest dynamic output currents are not greatly impacted by mismatches, according to the circuits' validation. Nearly 100% dynamic power efficiency is achieved by the mirror circuit because to its low dynamic power consumption.

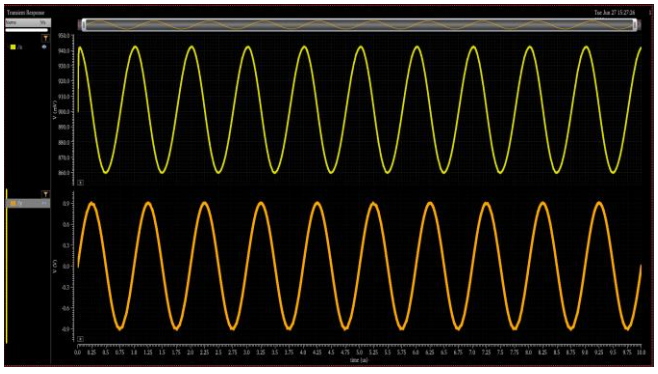


**Fig.6 Voltage Output Waveform of Class-AB Capacitance Multiplier**

| Parameters | Reference 1 | | Proposed work | |
|---|---|---|---|---|
| CMOS Technology (µm) | 0.18 | | 0.18 | |
| Structure | AB | | AB | |
| Base Capacitance C (pF) | 10 | | 10 | |
| Supply Voltage (V) | ±0.9 | ±0.25 | ±0.9 | ±0.25 |
| Multiplication Factor *k* | 11.4 | 10.88 | 11 | 10.55 |
| Power dissipation $P_{diss}$(µW) | 23.76 | 0.302 | 19.84 | 0.107 |

**Table 2 Comparison of Proposed Capacitance Multiplier to Recent Reference**

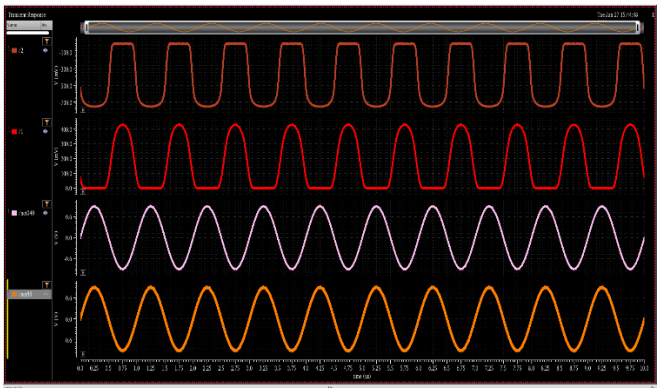


**Fig.7 Voltage Output Waveform of Class-AB Full-Wave Precision Rectifiers**

| Parameters | Reference 1 | | Proposed work | |
|---|---|---|---|---|
| CMOS Technology (µm) | 0.18 | | 0.18 | |
| Structure | AB | | AB | |
| $C_L$(pF) | 25 | | 25 | |
| Supply Voltage (V) | ±0.9 | ±0.25 | ±0.9 | ±0.25 |
| $R_L$ (Ω) | 150 | 150 | 150 | 150 |
| Power dissipation $P_{diss}$(µW) | 23.76 | 0.302 | 19.84 | 0.107 |

**Table 3 Comparison of Proposed Half -Wave Precision Rectifiers to Recent References**

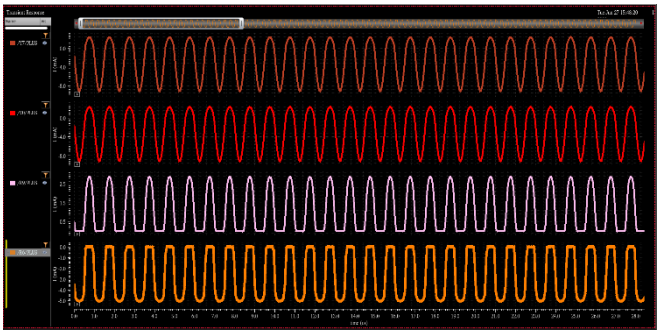


**Fig.8 Voltage Output Waveform of Class-AB Full-Wave Precision Rectifiers**

| Parameters | Reference 1 | | Proposed work | |
|---|---|---|---|---|
| CMOS Technology (μm) | 0.18 | | 0.18 | |
| Structure | AB | | AB | |
| $C_L$(pF) | 25 | | 25 | |
| Supply Voltage (V) | ±0.9 | ±0.25 | ±0.9 | ±0.25 |
| $R_L$ (Ω) | 150 | 150 | 150 | 150 |
| Power dissipation $P_{diss}$(μW) | 23.76 | 0.302 | 19.84 | 0.107 |

**Table 4 Comparison of Proposed Full -Wave Precision Rectifiers to Recent Reference**

## V. CONCLUSION

The study shows that the proposed circuits offer a solution for achieving higher performance in current amplification, capacitance emulation, and power efficiency in low-voltage operations. They effectively emulate larger capacitance, provide high output currents, and utilize a power-efficient current mirror architecture. The circuits are feasible for practical integrated circuit implementation and are suitable for power-efficient and voltage-constrained applications. Overall, they contribute to the development of more efficient and compact electronic systems. Class-AB current mirrors in CMOS technologies like 90 nm, 45 nm, and FinFET offer improved power efficiency and speed. Integration into SoC designs expands their applications to analog front-ends, sensor interfaces, and signal processing blocks.

## REFERENCES

1. J. Ramírez-Angulo et al., "±0.25-V Class-AB CMOS Capacitance Multiplier and Precision Rectifiers," IEEE Trans on very large-scale integration (vlsi) systems., vol. 39, no. 6, pp. 337–341, Jun. 2019.
2. Cosmin Radu Popa et al., "Improved Linearity CMOS Differential Amplifier with Low-Voltage Low-Power Operation," 6th European Conference on Electrical Engineering & Computer Science (ELECS) 2022 IEEE.
3. Deniz Özenli et al.,"A Grounded Capacitance Multiplier Circuit Employing VDTA," International Conference on Electrical and Electronics Engineering (ELECO) 2021 IEEE.
4. Natchanai Roongmuanpha et al., "CMOS Voltage Differencing Transconductance Amplifier with Linearly Adjustable Transconductance Gains," 5th International Conference on Engineering, Applied Sciences and Technology (ICEAST) 2019 IEEE.
5. Shashwat Singh et al., "Precision Capacitance Multiplier with Low Power and High Multiplication Factor ," 5th International Conference on Signal Processing and Integrated Networks (SPIN) 2018 IEEE.
6. F. Khateb et al., "Low-voltage fully differential difference transconductance amplifier," IET Circuits, Devices Syst., vol. 12, no. 1, pp. 73–81, Jan. 2018.
7. W. Germanovix et al., "Capacitance super multiplier for sub-hertz low-pass integrated filters," IEEE Trans. Circuits Syst., II, Exp. Briefs, vol. 65, no. 3, pp. 301–305, Mar. 2018.
8. Sagbas et al., "Component reduced current mode full-wave rectifier circuits using single active component," IET Circuits, Devices Syst., vol. 10, no. 1, pp. 1–11, Jan. 2016.
9. Christoph Tzschoppe et al., "Theory and design of advanced CMOS current mirrors," 978-1-4673-

9492-5/15/$31.00 c 2015 IEEE.
10. I. Padilla-Cantoya et al., “Enhanced grounded capacitor multiplier and its floating implementation for analog filters,” IEEE Trans. Circuits Syst., II, Exp. Briefs, vol. 62, no. 10, pp. 962–966, Oct. 2015.
11. M. Kumngern et al., “New versatile precision rectifier Montree Kumngern,” IET Circuits, Devices Syst., vol. 8, no. 2, pp. 141–151, Mar. 2014.
12. I. Padilla-Cantoya et al., “Low-power high parallel load resistance current mode grounded and floating capacitor multiplier,” IEEE Trans. Circuits Syst., II, Exp. Briefs, vol. 60, no. 1, pp. 16–20, Jan. 2013.
13. I. Padilla-Cantoya et al., “Capacitor multiplier with wide dynamic range and large multiplication factor for filter applications,” IEEE Trans. Circuits Syst., II, Exp. Briefs, vol. 60, no. 3, pp. 152–156, Mar. 2013.
14. Esparza-Alfaro et al., “Low-voltage highly-linear class AB current mirror with dynamic cascode biasing,” Electron. Lett., vol. 48, no. 21, pp. 1336–1338, Oct. 2012.
15. N. Minhaj et al., “OTA-based non-inverting and inverting precision full-wave rectifier circuits without diodes,” Int. J. Recent Trends Eng., vol. 1, no. 3, pp. 72–75, May 2009.
16. J. Aguado-Ruiz et al., “Three novel improved CMOS C-multipliers,” Int. J. Circuit Theory Appl., vol. 40, no. 6, pp. 607–616, Jun. 2012.
17. N. Minhaj et al., “OTA-based non-inverting and inverting precision full-wave rectifier circuits without diodes,” Int. J. Recent Trends Eng., vol. 1, no. 3, pp. 72–75, May 2009.
18. J. Choi et al., “High multiplication factor capacitor multiplier for an on-chip PLL loop filter,” Electron. Lett., vol. 45, no. 5, pp. 239–240, Feb. 2009.
19. J. Aguado-Ruiz, “Programmable capacitance scaling scheme based on operational transconductance amplifiers,” Electron. Lett., vol. 45, no. 3, pp. 159–161, Jan. 2009.
20. L.-C. Hwang et al., “Area-efficient and self-biased capacitor multiplier for on-chip loop filter,” Electron. Lett., vol. 42, no. 24, pp. 1392–1393, Nov. 2006.
21. J. Ramírez-Angulo et al., “Low voltage CMOS operational amplifiers with wide input-output swing based on a novel scheme,” IEEE Trans. Circuits Syst. I, Fundam. Theory Appl., vol. 47, no. 5, pp. 772–774, May 2000.
22. G. Di Cataldo et al., “Active capacitance multipliers using current conveyors,” in Proc. IEEE Int. Symp. Circuits Syst., vol. 2, May/Jun. 1998, pp. 343–346.
23. G. A. Rincon-Mora, “Active capacitor multiplier in Miller-compensated circuits,” IEEE J. Solid-State Circuits, vol. 35, no. 1, pp. 26–32, Jan. 2000.
24. S. Pennisi et al., “CMOS multiplier for grounded capacitors,” Electron. Lett., vol. 38, no. 15, pp. 765–766, Jul. 2002.
25. Y. Tang et al., “Adaptive Miller capacitor multiplier for compact on-chip PLL filter,” Electron. Lett., vol. 39, no. 1, pp. 43–45, Jan. 2003.