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# Simulation Model of Dual Boost Inverter Using Half Cycle Modulation Technique

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**Abstract**
The output voltage of conventional full bridge inverters is lower than the DC input voltage. In applications where the input DC voltage is very low, front end step up converters are typically needed, resulting in a two stage conversion process. The Dual boost inverter (DBI) offers many benefits, including fewer power devices, a straight forward design, and the ability to operate in both boost and buck modes. The traditional modulation technique used in DBI has a number of disadvantages, including the fact that all the devices work at higher frequencies and must tolerate larger voltage and current stresses, which increases conduction and switching losses and lowers efficiency. This study suggests a novel modulation technique called half cycle modulation (HCM), which makes all devices work at high frequency only every half cycle, significantly reducing conduction and switching losses and boosting DBI efficiency. Additionally, an improved DBI is suggested that can bypass the inductor current with little switching stress in order to reduce the current circulation losses in DBI. In this study, a detailed comparison between the traditional DBI and the HCM modulated DBI is discussed. In the MATLAB/SIMULINK software, the suggested DBI and its modulation techniques are simulated, and the results are also shown.

**Keywords:** Dual boost inverter, half cycle modulation, Voltage Stress

## 1. Introduction

The most popular arrange of elements to realise Dc-Ac power conversion is an A FULL-BRIDGE inverter. The output ac voltage is always less than the input dc voltage, which makes it appear to be a buck inverter. To achieve voltage step-up conversion in applications where the input voltage is low, an additional front-end dc-dc converter is needed [1], [2]. The efficiency is popularised by two stages, and the two-stage structure is complex in terms of system structure and controller design. The input voltage can be increased by using a line frequency transformer, but it will be bulky. Numerous single-stage inverters were developed to reduce the power components. suggested [3]-[9], which, thanks to its straightforward construction and low-power gadget, is advantageous to the enhancement of power density and efficiency. A quasi-single-stage inverter known as a Z-source inverter uses the passive network to raise voltage and permits shoot-through conditions in bridge legs [10, 11]. High Z-source capacitor voltage stress, a significant inrush surge, and a large number of passive components will all work against integration. A unique active buck-boost inverter that can boost voltage and carry out buck and boost conversion in a quasi-single-stage inverter has been proposed in Paper [12]. But there are too many power switches on this single-stage inverter.

Power supply for personal computers, office equipment, spacecraft power systems, laptops, telecommunications equipment, as well as DC motor drives, all make use of DC-DC power converters. A DC-DC converter's input is an uncontrolled DC voltage (Vg). The converter generates a controlled output voltage (V) that differs from Vg in amplitude and perhaps polarity. For instance, the 120V or 240V AC utility voltage in a computer off-line power supply is rectified to create a DC voltage of roughly 170V or 340V, respectively. The voltage is subsequently reduced via a DC-DC converter to the regulated 5V or 3.3V needed by the CPU ICs. Since inefficient power converters are expensive and difficult to cool, high efficiency is always necessary. The efficiency of the ideal DC-DC converter is 100%; in reality, efficiencies of 70% to 95% are frequently attained. This is accomplished by utilising chopper or switched-mode circuits, whose components dissipate very little power. The total output voltage can be controlled and regulated using pulse-width modulation (PWM). This method is also used in alternating current applications, such as high-efficiency AC-AC power converters, AC-AC power converters, and some AC-DC power converters (inverters and power amplifiers) (low-harmonic rectifiers).

The dual boost inverter (DBI), which is based on two symmetrical bidirectional boost dc-dc converters, was proposed in [3]. The DBI is made up of two boost converters with identical dc bias outputs that are sinusoidal voltages that are out of phase. Based on the step-up characteristic of a boost converter, the output voltage of DBI can be greater than the dc input voltage [13] – [15]. A waveform control was introduced in [16] to reduce the low-frequency ripple current. To increase its power bandwidth, a dynamic linearizing modulator-based boost inverter was suggested in [17]. Each group of the bidirectional boost dc/dc converters produces sinusoidal ac voltage with the same dc bias using the traditional modulation method [18]– [20]. However, under this modulation, all power switches of the converter function at a high frequency. This study suggests the half cycle modulation (HCM) technique, which involves switching between two boost groups so that each group outputs a voltage known as a "half-steamed bread-wave" with a dc bias. By contrasting the two outputs, the output side can obtain a clean sinusoidal ac voltage output. HCM can lessen the workload placed on switches and inductors by reducing the number of power switches operating at high frequencies. Switching and conduction losses as well as the core and copper losses of inductors can all be significantly decreased. Furthermore, a better DBI with two clamping switches is suggested based on HCM in order to decrease the current circulation loss in DBI. This work suggests the half cycle modulation (HCM) technique, which is used to create a DBI with two clamping switches. With low-stress clamping switches working in half cycle and line frequency, the improved topology can achieve increased efficiency.

This article suggests a Half Cycle Modulation (HCM) technique that operates two boost converters with the same DC bias, one during the reference wave's positive half cycle and the other during its negative half cycle. The output difference of two DC-DC boost converters is sent to the load as a pure sinusoidal voltage. The fundamental benefit of the suggested HCM technique is that it lessens the quantity of high-frequency power devices, further reducing the stress on switches and inductors from voltage and current. As a result, the core and copper losses of the inductor are likewise decreased, as are the switching and conduction losses of the switches. Additionally, an enhanced DBI is provided with two extra clamping switches and is additionally modulated using HCM in order to decrease the current circulation losses in

DBI. When compared to the traditional DBI, the upgraded DBI is more efficient and experiences less voltage stress.

## 2. Proposed Topology

The primary DBI circuit is depicted in Fig. 1, and the important waveforms used in conventional modulation are shown in Fig.2. A boost converter produces sinusoidal ac voltage with the same dc bias as its input. The following describes how the DBI converter functions while using a conventional modulation method. As depicted in Fig. 1, four power switches are all operating at high frequency (b). Let's define vo1 and vo2 as C1 and C2's respective voltages; Vdc is the offset voltage, Vin is the input dc voltage, $V_m$ is the output ac voltage's magnitude, and d1 and d2 are the corresponding duty cycles of Q1 and Q2.

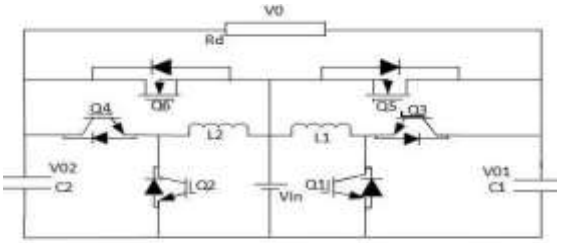



**Fig 1 Proposed Converter**

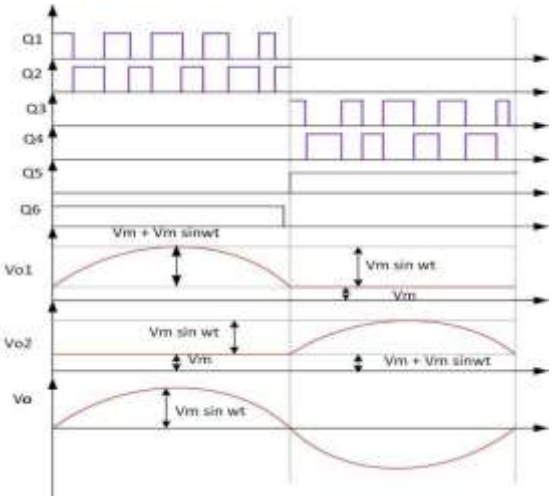



**Fig 2 Modulation strategy**

The following can be done to obtain vo1 and vo2 using the proper control logic:

$$v_{o1} = V_{dc} + \frac{1}{2}V_m sin(\omega t) - - - - - - (1)$$

$$v_{o2} = V_{dc} + \frac{1}{2}V_m sin(\omega t - \pi) - - - - - (2)$$

$$v_o(t) = v_{o1}(t) - v_{o2}(t) = \frac{V}{1 - d_1(t)} - - - - - (3)$$

Where $V_{dc} \geq V \quad + \frac{V_m}{2}$.

Form (1)-(3)

$$d_1(t) = \frac{\frac{V_m}{2} + \frac{V_m}{2}sin(\omega t)}{V \ + \frac{V_m}{2} + \frac{V_m}{2}sin(\omega t)} - - - -(4)$$

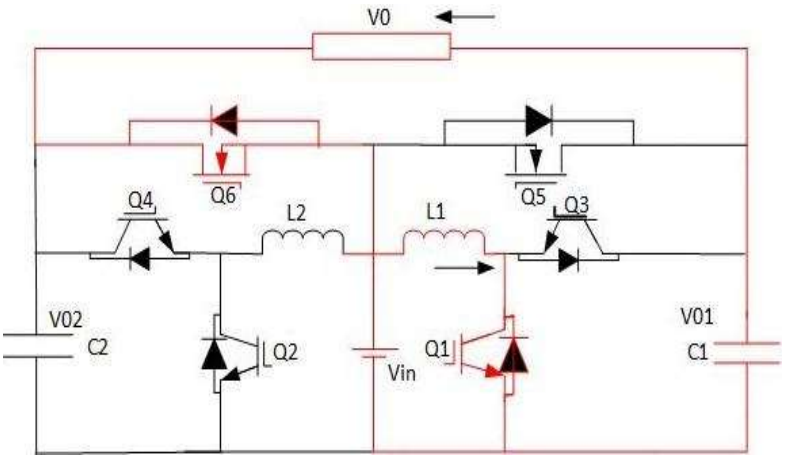
$$d_2(t) = \frac{\frac{V_m}{2} - \frac{V_m}{2}sin(\omega t)}{V \ + \frac{V_m}{2} - \frac{V_m}{2}sin(\omega t)} - - - -(5)$$

Form (1)-(5)

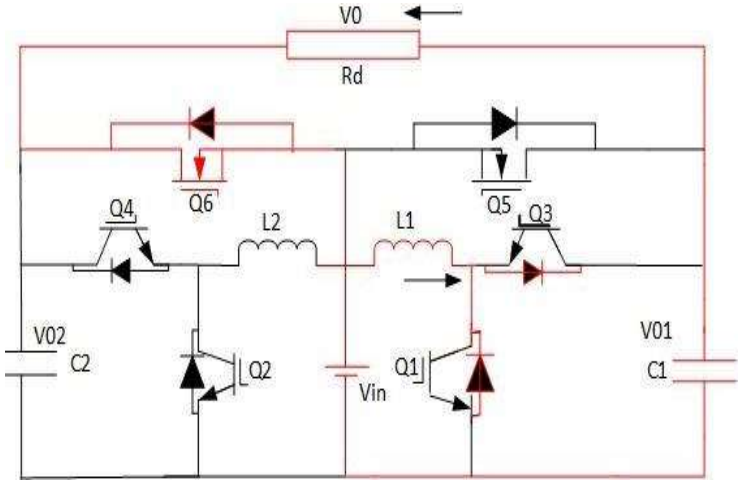
$$v_o(t) = v_{o1}(t) - v_{o2}(t) = V_m sin(\omega t) - - - -(6)$$

Fig.2 displays the waveforms of voltages vo1, vo2, and $v_0$ ; voltages vo1 and vo2 are sinusoidal with a dc bias. By varying vo1 and vo2, we can obtain sinusoidal output voltage ($v_0$). By varying, the output voltage $v_0$ produces a sinusoidal wave.

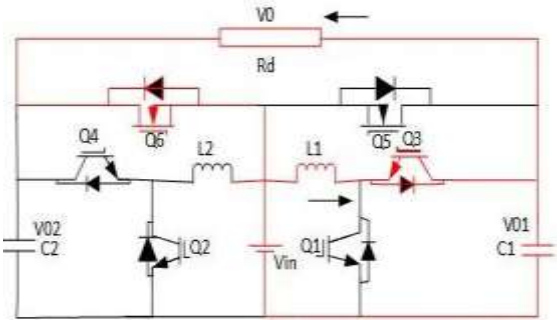
Fig. 3 depicts the suggested HCM strategy. Switches Q1 and Q3 operated at high frequency and in complementary fashion during the positive half cycle of the output voltage; Q2 was switched off; Q4 was turned on; the output voltage of capacitance C1 could be calculated as (7); and the voltage of C2 was Vin. Switches Q2 and Q4 operated with high frequency and in complementary fashion during the negative output voltage period; Q1 was switched off; Q3 was turned on; the output voltage of capacitance C2 could be calculated as (8); and



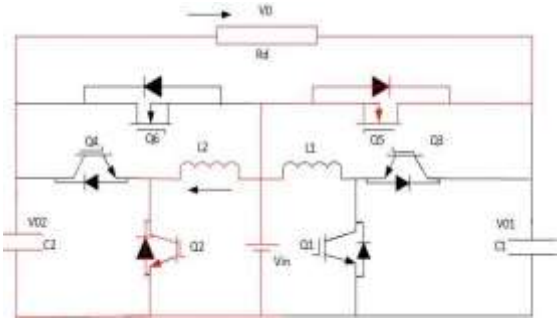

(a)



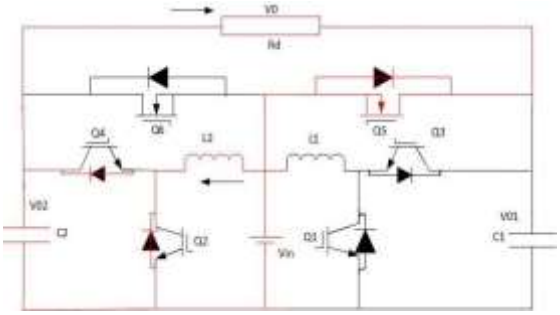

(b)



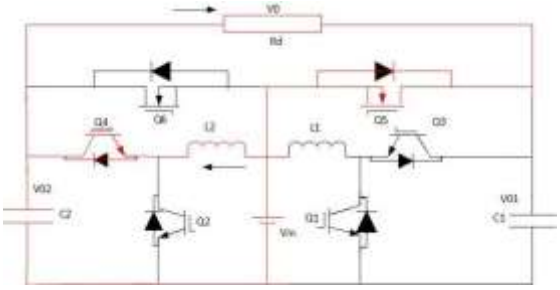

(c)



(d)



(e)



(f)

Fig 3 shows equivalent switching mode circuits. (A) [$t_0$, $t_1$], (B) [$t_1$, $t_2$] or [$t_3$, $t_4$], (C) [$t_2$, $t_3$], (D) [$t_6$, $t_7$], (E) [$t_7$, $t_8$], or [$t_9$, $t_{10}$] and (F) [$t_8$, t9]

$$\{v_{o1}(t) = V_m sin(\omega t) + V \quad v_{o2}(t) = V$$

$$v_o(t) = v_{o1}(t) - v_{o2}(t) = \frac{V}{1 - d(t)} - V \qquad (9)$$

Form (7)-(9)

$$d(t) = \frac{V_m sin(\omega t)}{V + V_m sin(\omega t)} \qquad (10)$$

Where the duty cycles of switches Q1 and Q2 are d(t). Calculating the difference in voltage between vo1 and vo2 will yield the load voltage.

$$v_o(t) = v_{o1}(t) - v_{o2}(t) = \frac{V}{1-d(t)} - V \quad = V_m sin(\omega t) \qquad (11)$$

The converter operating under HCM has four switching modes during a switching cycle. The control strategy for the HCM is shown in Fig. 3, and the corresponding circuits for the switching modes during the switching cycle are shown in Fig. . The following are some presumptions before the analysis that follows: All switches and diodes are perfect, all capacitors and inductors are perfect, and C1 = C2, L1 = L2 are all true. When the output voltage is positive:

1) State 1 [$t_0$, $t_1$]: At $t_0$, $Q_1$, $Q_4$, the input voltage, and the input current turn on. L1 is charged by the input current. As depicted in Fig. 4, load current (io) travels through $Q_4$(D4) to Vin, which is fluenced by C1 (a).
2) State 2 [$t_1$, $t_2$]: Dead time is the time frame. As illustrated in Fig. 4, at time t1, $Q_1$, $Q_2$, and $Q_3$ are switched off, $Q_4$ is turned on, and the current iL1 flows through $D_3$ or $D_1$ depending on the direction of the current (b). Through $Q_4$ ($D_4$), load current io travels to Vin.
3) State 3 [$t_2$, $t_3$]: $Q_3$ is activated at $t_2$, and iL1 flows through $Q_3$ ($D_3$). Through $Q_4$($D_4$), load current io travels to Vin. In Fig. 4, the current-flow path is displayed (c).
4) State 4 [$t_3$, $t_4$]: The same as mode 2, the period is also dead time, and the operational mode is the same. If the output voltage is negative at that time:
5) State 5 [$t_6$, $t_7$]: At $t_6$, $Q_2$, $Q_3$ are turned on, L2 is applied with the input voltage, and L2 is charged with the input current. According to Fig. 4, load current travels through $Q_3$($D_3$) to Vin, which is provided by C2 (d).
6) State 6 [$t_7$, $t_8$]: Dead time is the duration. As shown in Fig. 4, at time $t_7$, $Q_1$, $Q_2$, and $Q_4$ are all switched off, $Q_3$ is turned on, and the current iL2 flows through $D_4$ or $D_2$ depending on the current direction (e). Through $Q_3$ ($D_3$), load current io travels to Vin.
7) State 7 [$t_8$, $t_9$]: $Q_4$ is turned on at time $t_8$, and iL2 flows via $Q_4$ at time $t_9$ ($D_4$). Through $Q_3$ ($D_3$), load current io travels to Vin. In Fig. 4, the current-flow path is displayed (f).
8) State 8 [$t_9$, $t_{10}$]: The same as mode 6, the period is also dead time, and the operational mode is the same.

## 3. Results and Discussion

By simulating the proposed DBI with HCM in MATLAB/SIMULINK, the proposed low switching modulation technique is validated. This section presents the simulation findings. Table lists the simulation parameters utilised in this investigation (i). The switching signals for all four of the switches, which were produced using the HCM scheme and fed into the switches of the traditional DBI, are shown in Fig.4. It is clear from Fig 5, that all of the switches only function at high frequency for one half of a cycle. The duty cycle that is being thought about is 0.8.

**Table .I Simulation Parameters**

| Parameter | Value |
|---|---|
| Input voltage | 80 V |
| Output voltage | 110 V |
| Fundamental Frequency | 50 Hz |
| Switching frequency | 20 kHz |
| Inductance | 500 µH |
| Capacitance | 20 µF |

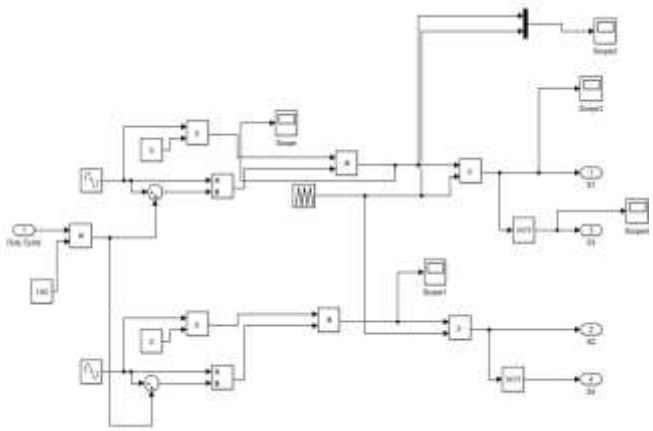


**Fig 4 Simulink Implementation of Half Cycle Modulation Technique**

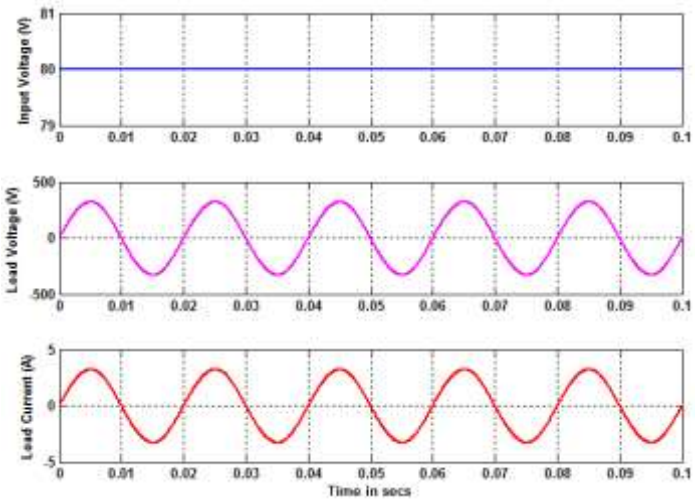



**Fig.5 Input DC voltage, Load Voltage and Half Cycle Modulation fed to conventional DBI**

The input DC voltage delivered into the traditional DBI is modulated through HCM in Fig. 3 (which is 80V DC). The standard DBI's load voltage and load current waveforms are also shown in Fig.5. It follows that both the load voltage and the load current are sinusoidal. Controlling the duty cycle of the switches will alter the load voltage RMS value. Increasing or reducing the duty cycle will consequently raise or reduce the load voltage; in this case, the duty cycle is taken to be 0.8.

## 4. Conclusion

In this article, an enhanced DBI with clamping switches was proposed. The HCM method with clamping switches of DBI maintains the benefit of buck-boost ability, per analysis and experimental results. Additionally, it has the advantages listed below over the original one: Comparing HCM to traditional modulation, just half of the switches are operating at high frequency, which obviously lowers the switching loss of the DBI. By using HCM instead of conventional modulation, the switches' voltage/current stress is reduced, further lowering the power switches' switching loss and conduction loss. HCM decreases the magnetic loss by lowering the inductor current. Switch clamping is useful for reducing the current circulation loss of the IGBT and inductor. It is also possible to lessen the circulatory current's conduction loss with low-stress MOSFET. Due to the reduced high-frequency switches

compared to classical modulation and lower inductor current stress, HCM can increase DBI efficiency. Additionally, the enhanced DBI can further increase efficiency due to the low conduction loss by adding low stress switches.

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