International Journal for Multidisciplinary Research (IJFMR)
E-ISSN: 2582-2160 ● Website: www.ijfmr.com ● Email: editor@ijfmr.com

Analog and Mixed-Signal Integrated Circuits of 5G and 6G Data Communication

Dr. C.T.K.Amarnath

Assistant Professor, Department of Computer Science, Pioneer Kumaraswamy College, Nagercoil.

ABSTRACT:
The complex analog and mixed-signal transceivers where overall system performance is often limited by the weakest performing subsystem. While analog and mixed-signal integrated circuits have significantly advanced, the future of 5G and 6G transceiver design could be accelerated by including artificial intelligence. In this combination, analog integrated circuit design and operation would harness machine learning to identify, characterize, and act upon variations and anomalies in system performance. Focusing on 5G and 6G, this paper investigates solutions for a unified intelligent integrated transceiver: a conceptual combination of a traditional analog subsystem, a supporting digital subsystem that enables artificial intelligence, and dedicated feedback circuitry or sensors that monitor performance, efficiency, or reliability. Active and passive components and propagation channels are reviewed based on their merits of introducing intelligence. Holistically and for broader applicability, the paper conceptualizes and coins the notion of an ‘‘intelligent integrated system (IIS)’’, which brings forward a novel unified vision and approach toward context-aware subsystems that dynamically interact with ambient and varying operating conditions. To demonstrate viability, the paper concatenates a select set of measurement results.

Keywords: Analog circuits, artificial intelligence, artificial neural networks, generative AI, electronic design automation, integrated circuits, intelligent integrated systems, machine learning, microelectronic circuits, 5G, 6G.

INTRODUCTION

Millimeter-wave (mm-wave) and Terahertz (THz) (a pro- visional frequency layer of 6G) electromagnetic (EM) waves enable broadband and low-latency telecommunications. Applications that utilize mm-wave frequencies are commonplace in integrated circuit (IC) communications, sensing, and security [1]. THz applications are also evolving into transformative solutions and reshaping telecommunications, imaging, and sensing [2]. Physics imposes stringent limitations on the propagation of high-frequency signals. Enhancements at the transceiver level are required to realize expected performance and efficiency of mm-wave and THz communication systems.

A conventional (non-configurable) transceiver is not capable of learning and predicting physics-based limitations. Signal attenuation, scattering, Doppler shift, and noise are fixed functions of the environment in which it operates [1]. Converting a conventional transceiver into a dynamic and adaptive system introduces the potential for real-time reconfigurability and performance enhancements. Artificial intelligence (AI) and machine learning (ML) advancement shows that computational algorithms can combine human intelligence, enabling automated and real-time optimization in transceiver systems.

The interface between the transceiver and the propagation channel is typically realized with passive

components. Using AI, a dynamic configuration could be created where feedback and adaptability would increase performance. While focusing on 5G and 6G telecommunications, this paper broadly introduces the notion of an intelligent integrated system (IIS). An IIS relies on reconfigurable active components and ‘‘smart’’ passive components. Advancements in reconfigurable intelligent surfaces (RIS) [3], [4], [5] allow for parameter adjustments and reconfigurability of meta-surfaces to adapt to variances in the propagation channel.

In this paper, the potential of applying AI and ML to active analog and mixed-signal microelectronics, combined with ‘‘smart’’ passive components, towards context- aware transceiver subsystems that dynamically improve high-frequency communication, is surveyed and presented. A simple, but deliberately extreme, analogy to consider here: a person is intelligent as a result of sensing, memory, brain power, and most importantly, continuous learning. Thus, the person delivers dynamic behavior, change and efficacy. IIS uses this notion.

A. CONTRIBUTION

This paper reviews the possibility to harness the full potential of previous, current, and future generations of microelectronic circuits through operational and artificial intelligence. The paper focuses on the potential to create context- aware systems through, among others, analog intelligent IC subsystems.

Configurable and context-aware transceiver subsystems can ideally adapt to operational variations to maintain or improve system performance. A separate intelligence-fed digital subsystem would adjust internal parameters to mixed signal components and rapidly react to changes in system behavior. At hardware-level, this is demonstrated in [6] and [7]. In both these articles, mixed-signal circuit behavior is influenced by external hardware or signal changes. The advantage of such a technique, in addition to traditional power/frequency adjustments, is that the transceiver could learn and understand why certain changes occur and in future react/predict internal changes in real-time. The information can be transferred or shared to accurately model performance variation. To extend the earlier analogy to further appreciate this behavior: in the ideal composition, within expected application behavior [8], IIS would incorporate Generative AI to integrated circuits and systems. Several academics have published research on mm-wave AI-assisted communications [9], [10], [11], [12]. This paper contributes to this research by providing a unified vision of these techniques. Additionally, this paper proposes that understanding, learning, adapting, and predicting the prop- agation channel can lead to further performance advantages within mm-wave and THz transceivers [3], [4], [5]

B. ORGANIZATION OF THE PAPER

Section II conceptualizes the IIS based on conventional telecommunications system. It provides a baseline for re- imagining wireless communications as adaptive intelligent systems.

Section III identifies and reviews subsystem-specific AI learning techniques in a wireless communications system.

Section IV identifies and reviews traditional reconfigurable transceivers in modern communication solutions.

Section V provides a detailed review of AI-assisted reconfigurable transceiver subsystems. It identifies crucial design parameters and how these can impact the system if paired with AI-assisted design.

Section VI describes true reconfigurability in wireless communications. It reviews techniques, considerations, and advantages of such a strategy toward realizing an IIS.

Section VII reviews mature enabling technologies in both the active and passive domains. The reviewed technologies enable present solutions and could be combined with AI to drive next-generation advancements.

Section VIII references the advances in mm-wave and THz-integrated technology through AI-assisted design and implementation. These results, if holistically unified, could potentially drive the realization of a true IIS solution.

Section IX, the conclusion, summarizes the findings in this paper.

II. CONCEPTUALIZING THE IIS

Fig. 1 is a visual comparison of the differences between a conventional telecommunications system and the IIS with intelligent ICs as its building blocks. In this paper, the reconfigurable IIS concept is also referred to as a *dynamic* transceiver.

In Fig. 1a the conventional transceiver relies on predetermined design parameters and ranged variables for its analog, mixed-signal, and discrete ICs. The transceiver has three primary components that determine its performance: the transmitter (Tx), the propagation channel, and the receiver (Rx).

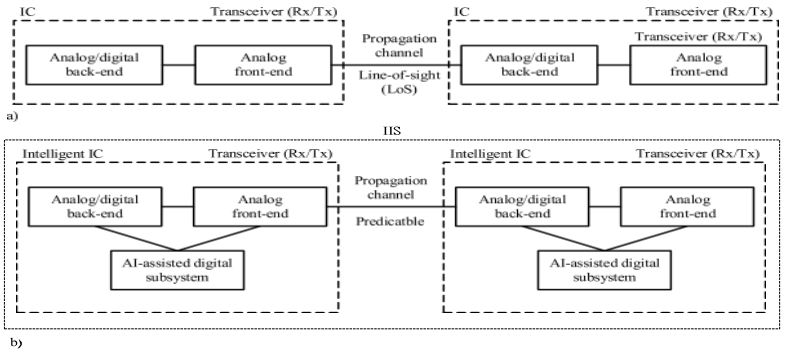

FIGURE 1. A comparison between a) conventional and b) dynamic (IIS) transceiver, also indicating the propagation channel.

Transceiver subsystems include frequency synthesizers, mixers, filters, amplifiers, modulators/demodulators, and antennas, thus a combination of active and passive components. The performance of the transceiver is governed by its weakest subsystem. However, free space path loss, scattering, and Doppler shift in the propagation channel introduces performance variations that are difficult to predict and mitigate. At mm-wave and THz communications, the key frequency candidates for 5G and 6G, the variations are significant as suggested by the Friis transmission equation [1]. Line-of-sight (LoS) and accurate directivity at these frequencies become increasingly crucial to maintaining performance without reverting to increasing the potentially unsafe transmission power.

Fig. 1b conceptualizes an IIS that is less dependent on LoS and that introduces additional feedback and feedforward loops through an AI digital subsystem. Its goal is to observe, predict, forecast, and adapt to operational and ambient variations. The AI digital subsystem is integrated into both the Tx and the Rx and relies on sensors, ML, and stored data to *reconfigure system parameters* as functions of real-time system performance. Additionally, in this representation, the *channel is reconfigurable* by introducing, for example, RIS, driven by programmable logic and powered by the AI digital subsystem(s).

III. AI-ASSISTED RFIC LEARNING TECHNIQUES

ML is a digital process that relies on computational resources to learn from its environment. It is scalable as a function of the resources used to train or infer ML algorithms. The speed of learning is proportional to the arithmetic capabilities of the neural processing units (NPUs) that execute numerous multiply-accumulate operations. Analog microelectronic ICs are not as scalable as many digital systems. They rely on transistor advances to increase performance by any order of magnitude. The scaling and improvement in transistor technology is a complex and expensive process and relies on longer-term generational advancements [13]. Increases in operation frequency govern subsystem-level performance and place limitations on both the efficacy of algorithms and how far IC technology can be pushed.

A. HIGH-FREQUENCY LIMITATIONS

AI-assisted analog radio frequency integrated circuit (RFIC) learning techniques depend on the target application and the intended subsystem. Not each intelligent IC subsystem in an IIS requires, or benefits from, the same learning technique. It is therefore important to identify, analyze, synthesize, and test numerous techniques for the most optimal solution. This modularity and customizability for different applications through programmability provides AI- assisted reconfigurable systems with an important edge over conventional systems. A level of ‘‘*softwarization*’’ of ICs allows for inter-application optimization.

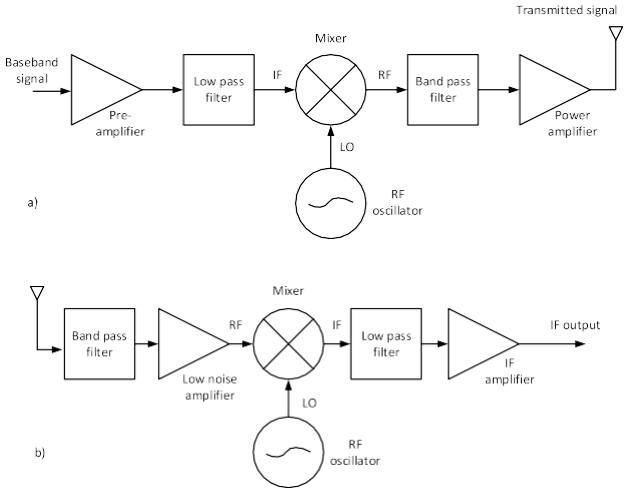

FIGURE 2. A simplified representation of the subsystems in an analog a) transmitter and b) receiver.

In a transceiver, each subsystem performs a predetermined task and its individual performance and efficiency impact the performance of the system. Fig. 2 is a simplified representation of the analog transmitter and receiver subsystems (adapted and simplified from numerous sources). It visualizes the core subsystems and components that would require intelligence to realize a truly intelligent system.

In Fig. 2, IF represents the intermediate frequency, and LO represents the local oscillator signal. Identifying and isolating the tasks of each subsystem in Figs. 2 a) and b) helps to determine their most effective learning technique. These techniques also depend on the format of the learning data, the sample size, and the available processing resources. At mm-wave and THz, these requirements will be different from lower frequency applications. In this context, primary differences between high and low frequencies include the following:

- More specialized modeling and optimization techniques are required at mm-wave and THz

subsystems to account for a larger number of parasitic effects.

- At mm-wave and THz operation, the bandwidth of each channel can be high and might require more complex signal processing techniques to extract the information. Learning techniques might therefore have to be adapted and become more complicated. In the ideal development, it would benefit from Generative AI.
- The propagation loss and LoS requirements at mm-wave and THz communication are significantly higher than for lower frequencies. As a result, related limitations may increase the complexity of learning techniques.
- Noise, scattering, and Doppler shift are typically more dominant in the receiver front end at mm-wave and THz transmissions. Therefore, modeling and optimization can become more complex in these systems. At the same time, adaptation would benefit from deployed intelligence.

TABLE 1. Machine learning techniques that can be applied to analog transceiver subsystems. The table contextualizes the contribution of this paper.

Learning technique	Baseband processing	RF-front end	Antenna (arrays)	EM interference	
GA*				×	
PSO*				×	
NN	×	×	×	×	×
CNN			×		
SVM			×		×
Random forest					×
AI and Generative AI				Contribution of this paper. The authors recognize that Generative AI, in particular, will create a number of challenges. [7] proposes mitigation by way of the ethically aligned design paradigm.	

*GA and PSO are optimization algorithms, or evolutionary algorithms, and are not machine learning techniques. However, these algorithms are included in this comparison since they are commonly used in conjunction with ML.

There are common learning techniques that apply well to mm-wave and THz-based analog transceivers. These methods can be adapted for a variety of applications, including:

- 5G/6G telecommunications,
- wireless backhaul,
- automotive radar,
- imaging and sensing,
- satellite communications,
- terrestrial point-to-point communications,
- wireless VR,
- unmanned aerial vehicles (UAVs),
- radio astronomy, and the
- internet of things (IoT).

Definitionally, to further inclusivity [14], 6G mobile phones may additionally incorporate satellite communication capabilities. It is envisaged that the trajectory towards 6G will need to be more inclusive than before [14]. This implies that there may be augmentation between frequency solutions (anticipated: higher frequency as well as satellite or other non-terrestrial solutions) [15]. Through inclusivity and the abovementioned applications, several applicable learning techniques can be identified, presented in the following paragraph.

B. HIGH-FREQUENCY LEARNING TECHNIQUES

The digital subsystem in an IIS would be responsible for maintaining and implementing learning algorithms. Eventually, the digital subsystem would perform Generative AI. In the current body of knowledge, references are available on applying AI and ML to mm-wave (and higher) frequency transceivers. Papers typically focus on individual (or a few for comparison) learning techniques and their modifications. This section summarizes the learning techniques that are typically applied to high-frequency systems. Providing an in- depth description of these learning techniques falls outside the scope of this paper but references are provided. A summary of common learning techniques that can be applied to transceiver subsystems is provided in Table 1. Furthermore, in Table 1, we contextualize the contribution of this paper.

From Table 1, it appears that genetic algorithms (GAs), based on adaptive heuristic or search engine algorithms, can be implemented in antenna array and RF front-end subsystem (mixers, filters, and amplifiers) algorithm development [16]. A GA typically performs better than random search algorithms since it uses historical data to lead the search toward the highest-performing region within the solution space. In [16], a GA is implemented to optimize the highly sensitive broadband silicon germanium (SiGe) heterojunction bipolar transistor (HBT) low noise amplifier (LNA) design methodology for radio astronomy. To perform adaptive equalization in analog RF front ends, neural networks are recommended since these tasks are typically applied to large datasets.

Baseband processing is performed by equalizers, decoders, and demodulators within a transceiver. This type of data relates to that of audio processing. Therefore, for adaptive equalization or channel estimation, neural networks and support vector machines (SVMs) are well suited. Convolutional neural networks (CNNs) and random forest estimation have been used for signal classification and modulation recognition.

GAs and PSOs can be used to optimize and improve the signal-to-noise ratio (SNR) in antenna arrays. For adaptive beam forming, neural networks that are trained on large datasets can give estimated

coherence factor weights and minimum variance to improve SNR.

EM interference signals are to be detected and classified during system operation. EM interference mitigation involves several stages, including the detection of unwanted signals through trained data. Once detected, several techniques can be used to mitigate the interference, including signal cancellation, beam forming, or spectrum sensing, all trainable by AI and ML. The techniques that are best suited for these types of operations include neural networks, SVM, or random forest estimation.

C. HIGH-FREQUENCY LEARNING IMPLEMENTATIONS

In implementing intelligence in each subsystem of a transceiver, analog high-frequency communication systems can be of benefit on several levels. For example, an AI- assisted analog RFIC benefits during both the design phase and the operating phase. For the design phase, AI datasets can contribute towards the electronic design automation (EDA). During the operating phase, continuously improving algorithms adapt, predict, and adjust circuit and system parameters to maintain or improve performance. Furthermore, for an IIS, and thus including intelligence in the channel, there could be further advantages in reducing complexity and cost and increasing sustainability and efficiency.

In [12] it is described how to select a learning technique for analog RFICs based on the target application and the size of the available dataset(s). Reference [12] suggests using the (unsupervised) clustering technique if processing resources are limited. This technique can provide results where relatively little information is lost. The second unsupervised technique suggested by [12] is principal component analysis, a linear approximation method that also requires less data, again without losing large portions of information. It is also suggested that the available datasets for a subsystem should first be determined, followed by the type of data generated at each level. To reduce dimensionality of complex datasets, [12] proposes linear discriminant analysis (LDA) which aims to maximize the separation between classes as opposed to maximizing variance. The decision tree, a clear distinction between the decision criteria and the outcome of the sequence of decisions, can be extrapolated from such results. Such a fast and highly scalable technique includes the Naïve Bayes classifier algorithm where the classifiers are relatively easily trained and do not require large datasets [12], hence a practical approach used by many researchers.

From a supervised training perspective, [12] suggests the SVM which has the advantage of quickly identifying the optimal linear data separators. However, its complexity in terms of output parameters can be difficult to interpret and apply. For large datasets and high volumes of information, it has been found that artificial neural networks (ANNs) and deep learning (DL) are popular techniques. These techniques use a single layer of linear threshold units (LTUs) and a weighted sum of its inputs, combined with a non-linear activation function to ‘‘achieve targeted design specifications while considering accurate physical properties of circuits and components’’ [12]. ANN and deep learning can possibly significantly reduce design time and simulation resources and account for variations in operation. In [12], an extensive list of contributions towards the modeling of analog RFIC components, subsystems, and systems is provided. In this paper, [11], [12], and [13] are referenced, resourced, and summarized.

The following section summarizes traditional adaptability and reconfigurability in analog transceivers, as opposed to AI-assisted techniques.

IV. RECONFIGURABLE TRANSCEIVERS

Reconfigurable or dynamic transceiver front ends that dynamically adapt their operating parameters to changing conditions have been presented in [15] and [23]. In this work, the subsystems rely on continuous

feedback and hardware configurability to progressively control performance at the component level.

A. HARDWARE FOR RECONFIGURABILITY

Reconfigurability can be achieved with a dedicated single- chip digital AI subsystem or through a system in a package (SiP). The merits of the latter are assumed, and an in- depth review falls outside of the scope of this paper. Before summarizing the most common methods that have been used to implement reconfigurability, the types of AI-dedicated hardware that can be used as a digital subsystem on an analog transceiver are briefly presented. These types include the:

- neural processing unit (NPU),
- graphics processing unit (GPU),
- field-programmable gate array (FPGA),
- digital signal processor (DSP),
- application-specific integrated circuit (ASIC), and
- tensor processing unit (TPU).

Each type of AI-dedicated hardware presents advantages and disadvantages that depend on the application (sub- system), power requirements, and data structures. Table 2 summarizes some of these advantages and disadvantages. Each subsystem would have its own power, space, and capability requirements, however, it is possible to consider more than one solution for a specific application within an IIS. In the infinitum, a deployed transceiver intelligence would be continuously updated using cloud/edge computing techniques. This would allow for enhanced usage of AI, particularly Generative AI.

When comparing the advantages and disadvantages from Table 2, it becomes evident that intelligent IC tasks in an IIS are application-specific and the choice of hardware is linked to certain trade-offs. If processing speed is important, the NPU, ASIC, and TPU are good candidates but can be expensive and may lack flexibility. The GPU and FPGA technologies are relatively mature. Related resources and tools are readily available for relatively quick and seamless integration. However, the power consumption of these devices is typically high. DSPs are optimized for signal processing and could be ideal for related subsystems, but they generally lack flexibility and AI algorithm support. In future, use of ‘light weight’ edge computing would enhance firmware integration.

B. TRADITIONAL METHODS OF RECONFIGURABILITY

To achieve current and conventional reconfigurability, software-defined radios (SDRs) can realize an analog sub- system and perform ‘‘corrective’’ signal processing on the transmitted or received RF signal. SDRs can dynamically alter subsystem behavior based on operating conditions but are limited by the input variables to observing, and adapting

TABLE 2. Some advantages and disadvantages of hardware that can perform intelligent subsystem operations.

Digital subsystem	Advantage(s)	Disadvantage(s)
NPU	Dedicated and optimized for AI Low power consumption	Limited flexibility
GPU	Mature hardware Many resources and tools are available	High power consumption Large form factor
FPGA	Highly customizable	High development cost Specialized skills required
DSP	Optimized for signal processing tasks Many resources and tools are available	Limited flexibility May lack AI algorithm support
ASIC	Dedicated and optimized for AI Low power consumption	High development cost
TPU	Optimized for TensorFlow® Open source	Limited flexibility
Edge/cloud-computing	Virtual update of firmware	Edge-computing is "light weight"

to, variations. SDRs and traditional reconfigurable antennas that modify mostly mechanical components such as switches and actuators have formed the basis of cognitive radio in its current form.

Cognitive radios can autonomously detect and adapt to their operating environment to optimize spectrum utilization and improve network efficiency [27]. Cognitive radios implement signal processing and intelligent algorithms to dynamically *sense and manage* spectrum disturbances. Although cognitive radios used as *dynamic* transceivers do present solutions to managing spectrum access, AI-assisted systems could potentially offer more flexibility in processing capabilities and better react to dynamic changes in the operating environment [22], [25].

A tunable filter can change its frequency and bandwidth parameters based on varying input conditions. This is typically achieved through adjusting input voltages and currents. These changes allow tunable filters to reject or accept specific frequencies over a relatively large frequency range. Tunable filters are, however, typically focused on accommodating multiple radio access technologies (RATs) and use RF microelectromechanical systems (RF-MEMS) to achieve reconfigurability [5], [28]. Enabling components of tunable filters include varactors (voltage-controlled variable capacitors) and switched capacitor circuits. The response of the filter can also be digitally adjusted by enabling or disabling capacitive configurations based on sets of series and parallel capacitor combinations. Through cascading multiple stages of tunable filters, it is possible to selectively switch between frequency and bandwidth requirements and enable transceiver reconfigurability. Tunable filters are most often used to vary operating configurations as opposed to mitigating variations in external factors. The number of filter variations is also dependent on the number of configurations that can be accommodated by the IC.

Capacitors, or varactors, are large components and the number of configurations is often limited by physical space. Furthermore, the number of logic configurations is also limited by the reprogrammable logic capabilities both on- or off-chip.

The voltage-controlled oscillator (VCO) is a key compo- nent for frequency synthesis in any transceiver and generates an analog oscillating signal based on a controllable input voltage. Reconfigurability of a transceiver can be achieved by adjusting the VCO control voltage to change the frequency band, or channel, of the transceiver. If the signal quality is poor, the VCO can adjust the carrier frequency to avoid interference and improve the SNR [15]. The VCO can also switch between modulation schemes to adapt to varying channel conditions or to increase transmission rates. There are however several limitations to using only the traditional VCO for transceiver reconfigurability. These include its limited frequency range, noise and phase noise performance impacts, power consumption, complexity, and stability. The VCO also operates independently from other transceivers in the environment and can potentially reconfigure towards a band that introduces interference to transceivers operating in its vicinity.

In mm-wave and THz operation, parasitic effects, propaga- tion losses, and LoS requirements are more prominent when compared to lower frequency transceivers. To mitigate the limitations of SDRs, tunable filters and VCOs to dynamically reconfigure transceiver parameters, AI-assisted reconfig- urable transceivers combined with RIS and/or intelligent antennas do present several advantages in performance and efficiency. The following section presents some AI-assisted approaches for transceiver subsystems with reference to existing research.

V. AI-ASSISTED RECONFIGURABLE TRANSCEIVERS

The premise of subsystem-level transceiver reconfigurability is not new, what is new, is introducing AI as the key feedback and learning system. With recent advances in AI as well as AI-dedicated hardware, improvements in these methods are actively being researched. To form an IIS as illustrated in Fig. 1b, an AI-assisted reconfigurable transceiver could integrate digital subsystems within the Tx and Rx transceiver ICs, intelligent antennas and RIS, to adapt to channel variations.

The following approaches at the subsystem level indicate the requirements and considerations at subsystem level, specifically considering data structures and typical parame- ters that require predictability and adjustment.

A. POWER AMPLIFIER

The linearity of a power amplifier (PA) is a key parameter which determines its performance based on its input and output signals. PA linearity, or P_{1dB} compression, indicates the maximum input power level at which the PA can provide a linear output signal while avoiding the compression region. P_{1dB} affects the gain, linearity, efficiency, third-order intercept point (IP3), and the noise figure of the PA. From a system-level perspective, the P_{1dB} compression point impacts both the dynamic range and error vector magnitude (EVM) of the PA. As reported in [7], at mm-wave frequencies, the PA is required to deliver a high and linear output power whilst maintaining efficiency. On scaled semiconductor technology and at a high operating frequency, external linearization may be required [29], such as predistortion.

Predistortion (analog or digital) is used to correct phase and gain distortions or to cancel out inter- modulation products. Predistortion relies on compensation coefficients that adjust the input signal before it is amplified to ensure linearity at the output. Predistortion coefficients are typically stored

and managed by a digital controller and their performance is related to the quality of the models. In traditional polynomial-based predistortion, the inverse gain model of the PA is represented by a limited number of coefficients. The performance results are reasonable but limited to the number and quality of the stored algorithms. Gain, phase, and temperature variations are typically monitored and adjusted for performance stability. Adaptive predistortion controllers [11] can detect nonlinearity in a system and iteratively adjust predistortion coefficients to minimize residual error. There are however second- and third-order problems that arise from this technique [11]. A key problem is that such a technique requires several iterations to converge to the nominal predistortion coefficients and during this time, performance can be degraded. This requires environment- specific data structures and algorithms to be stored for each successful steady-state condition, leading to increased storage requirements and latency during lookup. AI-assisted PAs rely on programmable and reconfigurable operations to adaptively optimize performance over antenna voltage standing-wave ratio (VSWR) variations [9] that lead to changes in the phase and gain of the PA [30]. By recon- figuring the gain and phase-offsets using the AI digital subsystem, improved linearity is obtained when external factors impact antenna VSWR [31]. AI-assisted optimization of P_{1dB} aims to mitigate performance degradation during operation through real-time machine learning in the dedicated digital subsystem [32]. Another important requirement is the use of complex modulation schemes such as quadrature amplitude modulation (QAM) in PAs to achieve high data rates. Using QAM requires the PA to process signals that are characterized by a substantial peak-to-average power ratio (PAPR). Introducing complexity into the design and optimization, the designer faces challenges. The PA can no longer rely only on load-pull techniques to achieve the desired performance at a specific output power level. This complicates the task of acceptable operation across a wide range of input power levels. Mm-wave and THz PAs can use power combining to achieve modest power levels. This creates a complicated impedance strategy during load-pull optimization. As a result, careful and tedious design of impedance networks is needed to ensure optimal power delivery. One approach to alleviate this is to utilize tunable transmission lines at the outputs of several parallel-combined PA cells to dynamically modulate the load impedance [33].

A future approach could entail a sizeable set of simulated data that is used to feed an algorithmic model to determine the effective load impedances at specific power points. Theoretically, this model should be able to determine the features of the design parameters that are not immediately obvious to the designer or the simulation tool. In the context of an AI-assisted PA, the operation demands utilizing a pre- trained model to control load-modulating circuit components. Furthermore, enhancing the efficacy of the model can be accomplished through the incorporation of empirically acquired data pertaining to temperature variations.

B. MIXER

The performance during baseband signal conversion to a required RF signal, performed by the mixer, affects system performance with respect to inherent trade-offs concerning conversion gain, noise figure, linearity, and isolation. These parameters impact the sensitivity of the transceiver, its dynamic range, and its noise figure. Mixer performance, energy efficiency, and form factor play a key role during its design phase, and numerous methods and techniques are used to optimize trade-offs. To achieve adaptability and reconfigurability of mixers, two primary methods are used, feedback and control as well as traditional design optimiza- tion through modeling and simulations. Like adaptive control systems in other transceiver subsystems, feedback and control monitors and measures the performance of the mixer

and controls parameters such as bias voltage and impedance, to adapt to variations in operating conditions. These digital subsystems are limited by their computing resources and the quality and number of algorithms. This adds significant cost and complexity to mixer design and implementation. Extensive design optimization and simulations lead to better- performing mixers under the intended operating conditions but are again limited by resources, time, complexity, and effort. Neither of these techniques allows predictive adaptive functions or improvement of the ‘‘statically’’ captured algorithms or design choices.

AI presents the ability to improve the performance of mixers by optimizing the mixer design and parameter selection through large datasets. These datasets aim to identify the optimal mixer topology, component values, and operating conditions for a given set of performance requirements. Such AI-assisted mixer designs can compare trade-offs from datasets in a relatively short amount of time that would otherwise not be possible for a human designer.

Learning how conversion gain, noise figure, linearity, and isolation are impacted in topologies and under operating conditions, while constantly learning from and improving the datasets can lead to improved performance, as reported by [16], [34], and [35]. As with feedback and control systems, AI-assisted mixers also require large and accurate datasets that may be difficult and time-consuming to generate.

C. FREQUENCY SYNTHESIZER

To generate an RF oscillation frequency, the frequency synthesizer is implemented using a stable oscillator, typically a VCO, and a phase-locked loop (PLL). At mm-wave and THz frequencies, the oscillator and PLL are impacted by limitations and performance degradations as a function of the high operating frequencies. Most notable and associated with high-frequency synthesizer operations is increased phase noise, and, since mixers require fairly high input drive, generating frequencies with sufficient power. This occurs due to high-frequency noise sources in both the oscillator and the PLL circuits. As a result, the increase in phase noise leads to frequency instability, and the sensitivity and range of the system are negatively impacted. High- frequency synthesizers also typically have higher power consumption due to the increased energy needed to maintain oscillation, higher parasitic losses, and significant transistor gate capacitances. Frequency synthesizers at mm-wave and THz frequencies cannot achieve the same levels of frequency tuning as lower frequency components due to the higher parasitic effects and limitations on the resonator quality factor. For reconfigurability through control voltage and varying frequency band of the VCO, AI-assisted configu- ration datasets are required to intelligently reconfigure the frequency synthesizer while maintaining operation integrity. Apart from using AI and ML to adapt to the operating environment, the frequency synthesizer also lends itself to benefiting from AI-assisted passive component design and reconfigurability. Although the frequency synthesizer traditionally benefits from the reconfigurability of internal voltages and currents, the effects, especially in mm-wave and THz operation, are limited. Introducing intelligence to the passive devices, both during the design and operating phase, assisted by AI-generated circuits and components, leads to more degrees of freedom in the frequency synthesizer. Furthermore, the oscillator in a PLL typically dominates the circuit simulation time. Due to the higher degree of nonlinearities the processing requirements for oscillators can be demanding. Behavioral modeling [10] can reduce the complexity and time of oscillator simulation, and continuous learning further increases performance without impacting the complexity, assuming adequate datasets.

At mm-wave and THz frequencies, low-noise VCO topologies are available, including cross-coupled,

LC, ring, injection-locked, coupled resonator, and subharmonic VCOs. Adding intelligence to these topologies may result in a time and cost reduction for designers. An ML technique for VCO design is proposed in [36]. The proposed VCO is process, voltage, and temperature (PVT) robust and has an expanded linearity range. A model is trained using an ML algorithm to predict the behavior of the VCO under various PVT conditions, resulting in a more robust and efficient circuit. The experimental findings reveal that the VCO has a greater linearity range and less phase noise than conventional VCO designs and enhances the efficacy of the integrated circuits.

In [35], VCOs are designed with high linearity and a wide tuning range by using neural networks to optimize the design. The Mamyshev oscillator cavity, which can produce high-energy ultrashort pulses based on the PSO algorithm is proposed in [37]. The experimental results showcase the effectiveness of the PSO algorithm, leading to a substantial enhancement in pulse quality and energy efficiency.

At high frequencies, HBTs are often used as the active components in VCOs. Through ANNs, the performance of these HBTs can accurately be predicted. The method for modeling the small-signal behavior of InP HBTs using ANNs is proposed in [38]. ANNs have the capability to offer precise predictions of device behavior without relying on extensive simulations or measurements. Moreover, ANNs possess the capacity to learn intricate relationships between input and output variables, enabling them to capture complex patterns. As noted in this paper, passive components behave differ- ently at mm-wave and THz frequencies due to higher parasitic effects. A neural network (NN) method for modelling and verifying the parasitic effects in RF and mm-wave IC designs is reported in [39]. It proposes an NN for modeling parasitic effects and extracting parameters from measurement data, employing a feedforward NN architecture and backpropagation algorithm. The proposed method is validated using multiple test cases and reportedly offers more accurate modeling and operating performance than existing methods. In addition, the potential for automated design optimization and parameter extraction from this method is discussed in [39]. Reference [36] presents a promising method for resolving the challenge of parasitic modeling and extraction verification in IC design using neural networks.

AI algorithms have the capability to explore an extensive design space for VCOs, effectively identifying dimensions and forms that maximize quality factors, minimize losses, and optimize component matching. Additionally, AI can forecast the performance metrics of passive components and VCOs, including quality factor, resonant frequency, and insertion loss based on their geometries, materials, and operating conditions.

D. MODULATOR AND DEMODULATOR

Modulation and demodulation techniques play an important part in transmitting, receiving, and correctly representing information. As the operating frequency increases, these subsystems increase in complexity due to the higher signal bandwidth, losses (both internal and external), and SNR. The need for improved and advanced modulation and demodulation techniques at mm-wave and THz frequencies has significantly increased. To avoid a continuous increase in complexity of both the circuits and algorithms, AI- assisted modulators and demodulators can alleviate these requirements. They can provide reconfigurability to mitigate (or replace) the proportionality of complexity and increased frequency. AI and ML algorithms that have learned and are learning from available datasets can adapt the modulation or demodulation scheme to optimize system performance [40]. As modulation schemes increase in complexity, power consumption also increases. The number of operations required to encode

or decode the information increases, leading to higher power consumption. As a result, the system power requirements also rely on the modulation scheme and can benefit from dynamically adjusting to a less complex scheme (if real-time operations or ambient conditions allow it). Furthermore, temperature and humidity that affect radio signal strength in outdoor wireless networks [41] could be used as an advantage. AI and ML algorithms that incorporate the requirements for transmit power and frequency diversity based on temperature and humidity can improve the efficiency of high-frequency outdoor communications.

Another benefit of using AI and ML in the modulation and demodulation process is the ability to extract data from the signal faster, if the model can recognize and predict the modulation scheme and the sequences to decode the information. For example, automatic modulation classifi- cation (AMC) [42] reportedly can detect the modulation scheme with lower overheads in the signal and identify suspicious or unwanted signal activities. In [42], AMC is achieved by extracting spectral features as a function of SNR to achieve 97% classification accuracy. Specifically related to 5G, [42] summarizes the algorithms associated to a combination of automatic modulation recognition (AMR- like AMC) and deep learning (DL) in the 5G physical layer [42]. The AMR likelihood ratio (LR), essentially a multiple-hypothesis problem, involves significant effort in constructing a likelihood function and selecting an appropriate threshold. Computing power is a limitation of this technique. According to [42], the feature-based (FB) recognition algorithm is a key enabler of AMR for low and accurate datasets. DL techniques are more robust than traditional AMC methods and often lead to more accurate results. DL is also a form of FB recognition; however, DL is capable of routinely extracting and classifying the features of the signal, based on prior information. Although there are numerous neural network deep learning techniques, according to [42] the CNN and the recurrent neural network (RNN) methods are popular for ANR. CNN consists of multiple convolutional layers, pooling layers, and fully connected layers [42]. Signal input features are extracted using the convolutional layers, while the pooling layer is used to downscale the high dimensionality of the convolution process. This can increase the speed of computation. The fully connected layer is used to combine extracted local features into global features and compute the classification. CNN works well with images and therefore can be applied as an AMR based on modulation constellation diagrams or eye diagrams. RNN uses recursive connections with feedback to the previous layer. The input to an RNN is information linked to time. Information is either classified as a valid input to the memory neuron, an output signal, or information that can be forgotten. Once decided, this information can be passed on to the next moment in time, where the process is repeated. As a result, RNN works well with audio, text sequences, and time series information. Since communication signals change with time, RNN can also be applied to modulation recognition. If sample size, or datasets, are limited, DL techniques have a lower likelihood of correctly identifying the modulation scheme and require forms of data enhancement or a combination of transfer learning and DL to overcome this limitation.

E. SUMMARY

Table 3 presents a summary of the performance variation(s) in analog transceiver subsystems as a function of reconfigurable parameters. To realize intelligent ICs, the digital subsystem would be responsible for analyzing and learning from these parameters to adapt and predict behavioral changes.

Transceiver subsystem	Performance variation(s)	Reconfigurable parameters
PA	Linearity (P_{1dB})	Predistortion coefficients
Mixer	Conversion gain, linearity, isolation	Bias conditions, topology (design phase)
Frequency synthesizer	Phase noise, frequency instability	Bias conditions, passive component reconfigurability
Modulator/ demodulator	Scheme performance, scheme complexity	Dynamic scheme adjustment, automatic recognition

TABLE 3. Analog transceiver subsystem performance variation(s) and the AI-assisted reconfigurable parameters to mitigate performance degradation. computational complexity and high accuracy. FB recognition in its traditional form also has limitations, evident in complex communication systems and if the SNR is low. Researchers still prefer using the FB recognition algorithms as a base for future development. The FB recognition method does not depend on reducing the likelihood function of a signal but classifies the scheme based on the classification accuracy of previous samples. Also, for the FB recognition method, the signal features must be appropriately chosen to create high-quality classifiers. In fading channels, this method struggles with fluctuations that can lead to incorrect identification.

AI-based DL presents itself as a good method in modu- lation and demodulation recognition, albeit requiring large The following section reviews the reconfigurability of front-end passive components to use channel intelligence and create an IIS.

VI. CHANNEL RECONFIGURABILITY

A popular research focus area of 6G transmission and THz frequencies is larger antenna arrays in multiple-input- multiple-output (MIMO) configurations. At both mm-wave and THz frequencies, signal transmission is largely bound to LoS and pencil beam transmissions. Conceptual architectures such as transmitting array antenna (TMA) and reflecting array antenna (RMA) [43] have played an important role in the manipulation of signal amplitude, phase, and polarization, specifically in wireless sensor networks (WSNs). In parallel with 6G research, RIS (also referred to as software-controlled metasurfaces) and integrated sensing and communication (ISAC) [5] have also received increased attention. These appear to have an ability to decrease (not eliminate) the requirement for LoS and compensate channel effects [44] without having to increase transmission power. To improve SNR [44], RIS-assisted MIMO uses many passive reflective units that adjust the phase of incoming waves and reshape the wireless propagation path in cases where LoS is blocked [28], [44] RIS can also vary in its shape (during the design phase), depending on the application [45]. RIS provides a LoS path for radar sensing, concentrates signal power on Rx [5] and moderates Doppler shift in vehicular communication systems [46] to increase data rates, efficiency, and stability. Its manufacturing cost can be considered lower when compared to implementing multiple base stations [28]. RIS capabilities can also be extended by amplitude-RIS (ARIS) and fully-RIS (FRIS) [47] towards increased channel orthogonalization. A brief description of these capabilities will be presented in this section.

As described in [45], RIS can be classified into three types, namely:

1. Reflector type, where the RIS only reflects incident signals towards Rx, on the same side of the base station.
2. Transmissive type, if the received/incident wave pene- trates the RIS and is transmitted to Rx on the opposite side of the base station.
3. Hybrid type, a combination of the above where the signal is split into a transmitted and a reflected portion.

Furthermore, according to [45], RIS is typically cate- gorized as either for wireless communications to improve spectrum efficiency, coverage, and energy efficiency, or for RF sensing to improve security, safety, and reliability. RIS also intelligently manages these types of networks [48] through software algorithms and analytical models. Fig. 3 is a simplified representation of a RIS propagation channel.

In Fig. 3, the transmitter and the receiver are intelligent ICs as proposed in Fig. 1b. The RIS in Fig. 3 is connected to an AI-assisted digital subsystem that continuously learns from data and information generated by the RIS. There are two signal paths demonstrated in Fig. 3. The first is the direct channel between Tx and Rx, or LoS, indicated by h_d . Secondly, the wireless channel from Tx to the n^{th} RIS element is denoted by $h_{A,n}$ and the component from the n^{th} RIS element to Rx is denoted by $h_{B,n}$, which constitute the signal components that can be dynamically adjusted through the RIS. The final expression for the transmission between Tx and Rx that originates from a vector sum of multiple paths is provided in [48].

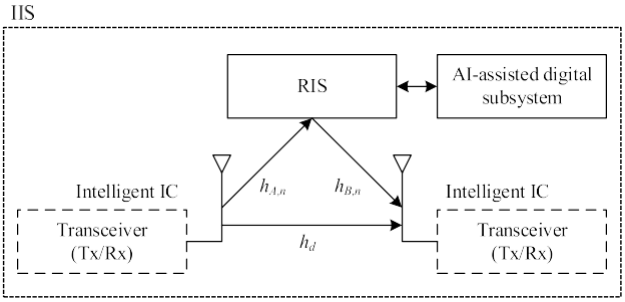

FIGURE 3. A simplified representation of a RIS propagateion channel.

From the simplified representation of a RIS propagation channel presented in Fig. 3, it appears that a combination of RIS and AI can result in intelligent propagation channels for both mm-wave and THz communications. Such a channel would rely on the ability of RIS to dynamically adjust the reflection coefficients of its individual elements, and as a result, vary the amplitude and phase of the EM wave that passes through it. AI can be employed to adaptively optimize the RIS configuration to maintain or improve certain performance metrics. The most common performance metrics that the RIS aims to optimize are SNR and bit error rate (BER). These performance parameters are typically influenced by - and to a higher degree for mm-wave and THz waves - physical obstacles, EM interference, or multipath fading. AI can therefore be used to continuously monitor the performance of the channel and intelligently adapt RIS configurations as the propagation channel fluctuates. Through AI integration in RIS, some key advantages are:

- Capacity and data rates can increase with the efficiency of the wireless communication system through opti mization of the RIS.
- Coverage and reliability can be increased by dynam- ically adapting to the immediate environment and reacting to physical obstacles or EM interference.
- Energy consumption of the wireless transceiver can be reduced by AI-assisted RIS through optimization of both power and bandwidth.
- Through intelligent transmission scheduling, energy consumption can be further optimized.
- RIS is a cost-effective solution when compared to more traditional techniques such as base station staggering.

By implementing AI, further cost reductions can be achieved as the requirement for more, or more

complex, antennas is reduced.

Although RIS presents several unique advantages for mm- wave and THz communications to be used in future 5G as well as 6G developments, there are also disadvantages and criticisms to be considered, namely:

- Integrating RIS and AI is a relatively complex task and requires skilled expertise to accomplish. Additional disciplines are required to implement such a strategy.
- Large datasets and sufficient processing capabilities are required to realize such a system. These datasets are typically generated over long periods of time.
- RIS (combined with AI) can improve wireless communication performance, however, for long-range communication, at mm-wave and THz, AI-assisted RIS would still be limited. Compared to massive MIMO, its superior ability to yield spatial multiplexing and reduce EM interference has not yet been proven.
- AI-assisted RIS, where algorithms are key, can lead to security concerns. Regulatory bodies will in time be required to evaluate the potential impact on privacy and security.
- The commercial and financial gains of using RIS need to be substantial for the trade and commerce industries to invest in and innovate in this space.

With regards to future 5G technologies and the development of 6G, AI-assisted RIS propagation channels remain a key enabling technology to achieve IIS.
In summary, the drive towards 6G transmission has focused on the utilization of THz frequencies and larger and more complex antenna arrays in MIMO configurations. At mm-wave and THz ranges, LoS, and pencil beam transmissions dominate, where concepts like TMA and RMA can manipulate signal properties. Innovations like RIS and ISAC leverage AI to mitigate LoS requirements and compensate for channel effects, enhancing signal quality and stability. RIS-assisted MIMO utilizes passive reflective units to optimize signal paths, while RIS can also take on various shapes during design. RIS, categorized for both wireless communications and RF sensing, is a cost-effective solution for improved efficiency, coverage, and energy consumption when integrated with AI. However, complexities and security concerns necessitate careful implementation. Ultimately, AI-assisted RIS emerges as a key enabler for achieving IIS in the context of future 5G and 6G technologies. To achieve reliable, efficient, and effective reconfigurability, the enabling technologies need to be identified and chosen based on various merits. This is an important step to realize intelligence in current (and ideally mature) technologies as opposed to relying on next generation implementations.

The following section reviews additional enabling technologies for reconfigurable transceivers.

VII. ENABLING TECHNOLOGIES FOR RECONFIGURABLE TRANSCEIVERS

This section provides a review of key technologies and methodologies of high-frequency communication systems, particularly in the context of 5G and the forthcoming 6G land- scape. It reviews the possibility of intelligently harnessing EDA tools and using AI for active and passive component modeling, circuit synthesis, and optimization processes. This can lead to enhanced design quality, reduced cycle times, and lowered engineering and manufacturing costs, potentially at the cost of dataset generation and skills development. Moreover, this section provides another brief survey of RIS with AI

integration specifically towards spectrum efficiency, improved coverage, and energy consumption. Finally, the concept of softwarization for dynamic adaptation in 6G access networks and harnessing AI, SDN, NFV, and cloud computing principles is reviewed and presented. The following paragraph introduces the concept of AI and ML in EDA tools.

A. EDA TOOLS

Incorporating AI into analog RFIC design can bring sig- nificant advantages when leveraging EDA tools. EDA tools can perform component modeling, circuit synthesis, and automated optimization. These tools enable the comparison of various architectures and design parameters, for example transistor sizes and biasing, to achieve optimal efficiency and desired performance levels. EDA tools with AI capabilities should simultaneously reduce the duration of the design cycle and improve the design quality, lowering the cost and increasing yield. Moreover, these tools reduce reliance on scarce and costly analog IC design skills, mitigating the challenges associated with skill availability in the field. The performance of analog ICs is related to multiple parameters that can be interdependent and competing. AI algorithms could optimize these parameters beyond the limitations of traditional methods, offering the optimal settings necessary to achieve the desired functionalities of the transceiver.

The design flow and EDA tools for analog design are typically complex and the design phases are correlated [49]. Several design tasks, such as partitioning, floor planning, placement, routing, and compaction are manual processes. Limitations in EDA tools and the large number of interde- pendent design parameters add to the complexity of analog design. The conventional approach to analog modeling and design involves reducing complexity through circuit parti- tioning, assuming that certain dependencies are negligible, and focusing on the most significant ones. It also typically assumes linearity in the circuit. This approach can result in suboptimal and simplified designs. Considering many architectures and the effects of various design parameters and nonlinearities on performance, AI algorithms and datasets can potentially achieve optimal and efficient designs.

Integrating these datasets into EDA tools is, however, time consuming and in many cases, application specific. The success of AI and ML methods depends on diverse and sizable training data sets. Reference [50] reports a dataset of ∼2 million simulations to train a generative neural network.

While it is desirable to obtain vast amounts of data, computational burden could also be a limiting factor. Several methods, such as online learning [51] and transfer learning [52] have been proposed to alleviate this challenge. Another critical aspect for AI and ML implementation is choosing appropriate tools. Practical computational constraints (such as the lack of large datasets) could rule out neural networks. Conse- quently, other ML tools such as Kriging and support vector regression have gained attraction and yielded successful results [53].

Modern EDA tools and designers do not yet take full advantage of AI-assisted designs as these datasets and their integration into EDA tools are still developing. Research on analog synthesis using the genetic algorithm (GA) can be traced back to the 2000s [54]. Approaches of generating circuit netlists using the GA and circuit-building languages were proposed [55], [56]. Other approaches in the synthesis of linear and nonlinear circuits are found in [57], [58], and [59], and a list of papers on GA-based optimization is given in [60]. As partitioning, floor planning, placement, and routing tools as earnable multi-objective evolutionary algorithms and AI have become major research topics, EDA tools based on ML are expected to grow.

B. ACTIVE COMPONENTS

A core component in any transceiver, and in any IIS, is the transistor, the primary active component that determines the switching speed of the circuit. The switching speed of the transistor is a function of its underlying technology (material and size, for example) and its electrical properties. Achieving mm-wave or THz wireless communications is not possible if the transistor is not capable of switching at the desired speeds. As the transition to 6G provisions for THz telecommunications, identifying the potential enabling active components is key. Since the compounded semi-
($Si_{1-x}Ge_x$) transistors are reaching f_T above 1 THz and conductors indium phosphide (InP) and silicon germanium f_{max} above 2 THz, these technologies present themselves
as underlying technologies for new-generation wireless networks. The following paragraphs further explore enabling active components, with no specific mention of AI or ML in its development.

To quantify the viability of a transistor as an enabling technology in high-frequency (mm-wave and THz) operation, some key parameters should be considered. Importantly, it is not always practical to solely consider performance parameters, but external factors should also be included such as cost, complexity, availability, and reliability. A rel- atively straightforward and electrical approach to defining a transistor is by looking at its transition frequency, f_T, its maximum oscillation frequency, f_{max}, and its collector- emitter breakdown voltage (BV_{CEO}). f_T is the frequency where the current gain of the transistor reaches unity [61], therefore where the transistor can be used as an amplifier with linear current gain (typically in the common-emitter configuration to achieve its maximum frequency response). f_{max} is the frequency where the power gain of the transistor reaches unity, therefore the maximum frequency where the transistor can be used as an oscillator or frequency multiplier (typically in the common-base configuration to achieve maximum power). BV_{CEO} describes the maximum voltage that a transistor can withstand across its collector- emitter junctions before breakdown occurs, a function of its doping concentration – therefore an important parameter to describe its power handling capabilities. f_T and f_{max} (typically, f_{max} is higher than f_T) can be verified in harmonic distortion analyses and power and noise figure measurements [34]. Silicon has dominated microelectronic circuits since 1965 and as a result, has also been extensively researched ever since. If maturity is the primary consideration, silicon technology nodes are the most common. However, silicon does not have the best performance for high-frequency wireless communications, especially when considering the demands of current and future wireless solutions. Compound semiconductors, specifically III-V compounds, such as GaAs, InP, and SiGe alloys, have already (since 2000) demonstrated superior high-frequency performance as well as additional unique properties, albeit they are not as mature as pure silicon. Increasing research into these technologies and a rapid drive toward their maturity have made these alloys more viable alternatives in mm-wave and THz wireless communications. SiGe active components, particularly the HBT, are a highly feasible candidate for high frequency (mm-wave and THz included), high bandwidth, and high data rate wireless communications. The alloy, formed by adding germanium to silicon during the material processing phase, increases the carrier mobility, decreases noise during operation, and increases the cutoff frequency of the transistor, as has been presented in [7], [16], [34], [62], [63], [64], and [65]. The bandgap and electron mobility of $Si_{1-x}Ge_x$ depends on ranging between pure silicon ($x = 0$) and pure germanium (x the material composition and doping level of the material, = 1). At $x = 0$, the bandgap and electron mobility are 1.12 eV and 1400 cm^2/V.s, whereas at $x = 1$, these are 0.66 eV and 1900 cm^2/V.s, respectively. As a result, its ability to operate at higher frequencies when compared to traditional silicon and its higher gain at lower power consumption has spearheaded SiGe towards

becoming more mature. SiGe transistors are promising for use in 6G communication systems. SiGe transistors can be integrated with silicon components on-chip, also referred to as BiCMOS technology, and enable complex and highly integrated circuits at high-volume production. There is, however, more research required to determine the long-term maturity and validity of SiGe as an enabling technology in 6G communications. In [62] a SiGe HBT with f_T, f_{max}, and BV_{CEO} of 505 GHz, 720 GHz, and 1.6 V is presented by optimizing the vertical profile of the HBT in comparison to earlier technologies presented by the same authors. As an industrial process, the progress presented by [62] shows a significant concept for next- generation SiGe HBTs and is an enabling technology in future wireless communications. Comparative f_T and f_{max} in CMOS are presented in [63]. In TCAD, [63] compares the fin-shaped field-effect transistor (FinFET) with the nanosheet FET (NSFET) in terms of its analog RF applications. The transistors are designed through a carefully controlled 5 nm gate-length CMOS transistor with a dual channel structure and a high-k/metal gate stack. The NSFET in [63] presented a f_T and f_{max} of 441 GHz and 604 GHz, whereas the FinFET was 413 GHz and 555 GHz, respectively. Also considering its noise and power handling capabilities, [63] found that the NSFET CMOS transistor was superior. When comparing the outcomes presented in [63] to the current capabilities of SiGe, although these are comparable in performance, it should also be noted that the CMOS NSFET is not necessarily representative of its real-world performance. Furthermore, the complexity and cost of the transistor in [63] are likely to be higher than that of a SiGe HBT.

InP is another III-V compound semiconductor that presents as a promising high-frequency, low-noise, high breakdown voltage technology for use in mm-wave and THz-based wireless communications. InP inherently supports high carrier transport and low parasitic capacitances with its 1.35 eV direct bandgap and 5000 cm^2/V.s electron mobility at room temperature. InP additionally presents thermal and mechanical properties that enable it to be used in high- temperature and high-power applications. InP-based high electron mobility transistors (HEMTs) have also demon- strated superior noise performance and power density. These characteristics are key in both low-noise amplifiers (LNAs) and power amplifiers (PAs). In [65] a double HBT and in [64] a single HBT InP-based transistors are presented with f_T of 428 GHz and 509 GHz, respectively.

C. PASSIVE COMPONENTS

In the passive domain, the focus of this paper largely centers around the innovative integration of RIS, a critical facet in the realm of high-frequency communications. The utilization of RIS in conjunction with AI promises transformative enhancements in terms of spectrum efficiency, coverage, and energy consumption. By dynamically adjusting reflection coefficients, RIS intelligently shapes propagation paths, mitigates performance degradation due to obstructions or interference, and adapts to the immediate environment. This amalgamation of RIS with AI can amplify wireless communication capabilities, while also presenting potential cost savings compared to traditional methods. The pivotal role of AI-assisted RIS propagation channels in achieving IIS is underscored in references in this paper and reviewed in the previous section.

D. SOFTWARIZATION

6G access networks are expected to serve large numbers of distinct devices with traffic of up to 1 Gbps per square meter and latencies as low as 0.1 ms. Numerous human-type and machine-type applications are envisioned, each with its own quality of service (QoS), traffic, security, and latency

requirements. As an example, robotic surgery necessitates high reliability and low latency, while unmanned vehicle applications rely on seamless and rapid handovers. The system intelligence in the edge network and end devices cannot remain static due to significant and dynamic variations in wireless communication channels (such as the impact of blockage in small cells at mm-wave frequencies), traffic types, reliability considerations, user behavior, device mobility, energy consumption, and cybersecurity require- ments. 6G supports the concept of connecting intelligence rather than connecting objects to achieve high efficiency, flexibility, portability, and automation. This results in high levels of computing and ML in edge networks. The range of communication scenarios in such a network is virtually boundless, making it impractical to address them effectively with ‘‘static’’ software solutions. Therefore, the concept of *softwarization* emerges as a solution [66]. This concept, along with virtualization, distributed intelligence, and ultra- densification, is already available in 5G networks [66]. *Softwarization* combines SDN, network function virtualiza- tion (NFV), and cloud computing (CC) principles.

Softwarization is a new concept of intelligence in 5G and 6G networks, specifically related to its ability to adapt to its environment (communication channel, interference, obstacles, mobility), applications, and other dynamic changes within the network. To enable rapid adaptation, AI models should be capable of making fast decisions without the need for supervised training. They should possess the ability to adapt to dynamic environments and converge swiftly. Moreover, the hardware infrastructure should be programmable, allowing on-demand downloads for optimiza- tion and integration of intelligent modules. Such modules consist of optimization software and AI modules. In future, these modules could be cloud/edge-computing enabled and constitute Generative AI capabilities.

SDN allows decoupling the network control plane from the data plane [67] (control functions are centralized and withdrawn from the infrastructure), while NFV separates design, deployment, and management functions from propri- etary hardware. AI implementation in edge networks offers the advantage of offloading computations and storage from a centralized cloud. This approach enhances bandwidth and reduces latency since edge networks are in closer proximity to end devices. Additionally, storage and processing of private information in edge networks rather than com- mercial clouds can reduce potential security risks. Certain computer and storage-intensive AI and ML algorithms can still be handled by a centralized cloud. The SDN, NFV, and CC principles enable high flexibility, efficiency, automatic network management, and on-demand resource provisioning [68].

A software-based high-level architecture is proposed in [66] where ML is performed by multi-armed bandit (MAB) algorithms. This architecture is structured into three layers: the data plane, the control plane, and the application plane [66]. The data plane encompasses diverse network infrastructures like base stations, wireless LAN access points, and end devices such as sensors, IoT devices, and user terminals. The control layer houses GPUs for parallel processing of software modules within the application layer. Within the application layer, optimization and AI modules for various applications are deployed. These modules handle tasks such as network resource allocation, quality of service (QoS), and optimization algorithms for both edge networks and end devices.

The architecture in [66] is versatile and provides better performance than in cases where AI is embedded in various devices, such as in [69]. This architecture is validated by simulation in two scenarios based on MAB algorithms: neighbor discovery and selection (NDS) in a device-to-device (D2D) network as well as in an aerial gateway selection in a UAV network [69].

Various research teams have presented and proposed solutions that address intelligent adaptations of accessible technologies. The following section highlights some of these advances.

VIII. ADVANCES IN MM-WAVE AND THZ ICS

Mm-wave and THz integrated technology has significantly evolved over the past decade, advancing telecommunications, sensing, and imaging. This section presents a review of the transceiver technologies and strides made in AI and ML to bridge the ‘‘THz gap’’ and the complexities of signal generation and detection in the 0.1–3.0 THz frequency range. Collaboration between electronics and photonics is crucial to harness the potential of THz integrated systems. The THz gap, a domain between microwave and optical frequencies, has suffered from inefficient signal generation and detection methods. Laser-based technologies, utilizing femtosecond lasers and lightwave-to-THz converters, have created new integration possibilities and renewed interest in mm-wave and THz ICs. While these techniques have been successful, their bulkiness and high costs have necessitated compact and efficient chip-scale THz solutions [70].

For example, dynamic waveform shaping has emerged as a transformative tool for reconfigurable radiated periodic signal generation with picosecond time widths [71]. This technique allows for precise manipulation of THz (input) waveforms and enables adaptable signal synthesis. An illus- trative example of this advancement is found in a scalable architecture presented in [71]. This architecture generates and radiates sub-THz periodic waveforms by combining radiated EM fields of fundamental and multiple harmonic frequencies. By controlling the amplitudes and phases of these harmonics, sharp pulses with picosecond time widths can be dynamically shaped in free space, enabling high temporal precision [72]. This advancement holds significant potential for applications requiring ultra-fast and reconfig- urable signal generation, underscoring the interdisciplinary synergy between waveform engineering and THz-integrated technology. Furthermore, by converging disciplines such as ‘‘solid-state and photonic devices, 2D materials, het- erogeneous integration, and system demonstrations’’ [73], researchers have already developed multifunctional and reconfigurable architectures [73]. The focus of THz devices has shifted towards more holistic system-level properties, promoting versatility and programmability.

Silicon-based technologies, exemplified by CMOS and SiGe, offer high integration levels but encounter limitations in THz frequency performance (f_{max}). In contrast, III–V devices such as InP-based HEMTs and HBTs have excelled in power generation beyond the 1 THz threshold. SiGe-based devices show promise for future improvements in f_{max}, potentially exceeding 1 THz, while heterogeneous solutions combining III–V and silicon are envisaged for higher frequencies [73].

The future landscape of THz integrated systems is defined by emerging applications that hold transformative potential. THz imaging and sensing hold promise for non-destructive quality control, 3D imaging, radar, and gesture recognition [74] across diverse sectors. These applications demand compact, efficient, high-performance sensing devices, positioning integrated circuit technology as a pivotal enabler [74]. THz applications center around the development of reconfigurable chip-scale systems capable of spectrum, radiation pattern, and polarization manipulation. For example, THz spectroscopy offers the potential for advanced chemical composition identification. According to [74], AI and ML could advance real-time THz imaging applications, especially in the 100–300 GHz range, and benefit from computational-based integrations [74].

THz integration extends to wireless communications, with prospects for wireless backhaul, data centers, short- range high-bandwidth links, and satellite communication. Challenges related to ‘‘circuits and communications archi- tecture, channel estimation, and resource management’’ drive innovation [75].

In summary, the landscape of THz integrated technology has undergone a profound transformation. Recent advances have propelled the field beyond historical limitations, paving the way for diverse

applications in telecommunications, sensing, and imaging. As interdisciplinary collaboration continues and challenges are addressed, the future of THz integrated systems holds great promise for reshaping multiple industries. The incorporation of dynamic waveform shaping techniques further enhances the potential for reconfigurable signal generation, adding a new dimension to the capabilities of THz integrated technology.

IX. CONCLUSION

Analog transceivers operating at mm-wave and THz fre- quencies are important within the context of 5G and 6G telecommunications. This has ushered in a new era of challenges and opportunities. These frequencies enable broadband, low-latency telecommunications, but have inher- ent limitations, such as high propagation losses, high cost, and complexity. Conventional transceivers could adapt to a dynamic environment and harness the full potential of high frequency bands if design and operational intelligence is introduced. This paper presents a novel and unified survey of intel- ligent analog transceiver subsystem capabilities. To address transceiver subsystem limitations at high-frequencies, this paper reviews research on AI and ML integration into analog and mixed-signal microelectronics. By equipping analog transceivers with operational intelligence through digital subsystems, it points to the possibility of creating intelligent transceivers. Such ICs would be characterized as configurable and context-aware transceiver subsystems that adapt to variations in performance to maintain or enhance system efficiency. This system would have the capacity to learn, understand, predict, and react to real-time environmental and operational changes. System adaptability and reliability could therefore be improved without more expensive and complex technologies, harnessing the full potential of current implementations.

Furthermore, our proposal extends beyond the confines of the transceiver itself, recognizing that the propagation channel, often interfaced through passive components, plays a crucial role in system performance. By introducing intelligence into these interfaces, passive components would dynamically adjust to variations in the propagation channel, and it could be possible to realize a true IIS.

Finally, the implementation of intelligent and reconfig- urable active and passive components can reduce analog design complexity and potentially lower the cost of realizing next generation systems. As a unified approach, with significant impetus of cloud/edge computing and Generative AI, the paradigm would revolutionize the approach towards mm-wave and THz transceiver design, ensuring efficient, reliable, and adaptable communications. Recognizing that Generative AI has societal implications, this paper refers to prior work on ethically aligned design. In the broader notion of IIS, including 5G and 6G, intelligence must remain within this societal bound.

REFERENCES:

1. J. Lambrechts and S. Sinha, Microsensing Networks for Sustainable Cities, vol. 18. Cham, Switzerland: Springer, 2016, doi: 10.1007/978-3-319- 28358-6.
2. A. Leitenstorfer, A. S. Moskalenko, T. Kampfrath, J. Kono, Castro-Camus, K. Peng, N. Qureshi, D. Turchinovich, K. Tanaka, G. Markelz, and M. Havenith, ‘‘The 2023 terahertz science and technology roadmap,’’ J. Phys. D, Appl. Phys., vol. 56, no. 22, Jun. 2023, Art. no. 223001, doi: 10.1088/1361-6463/acbe4c.
3. S. Venkatesh, X. Lu, H. Saeidi, and K. Sengupta, ‘‘A programmable terahertz metasurface with circuit-coupled meta-elements in silicon chips: Creating low-cost, large-scale, reconfigurable terahertz

metasurfaces,'' IEEE Antennas Propag. Mag., vol. 64, no. 4, pp. 110–122, Aug. 2022, doi: 10.1109/MAP.2022.3176588.

4. S. Venkatesh, D. Sturm, X. Lu, R. J. Lang, and K. Sengupta, ''Origami microwave imaging array: Metasurface tiles on a shape-morphing surface for reconfigurable computational imaging,'' Adv. Sci., vol. 9, no. 28, Oct. 2022, Art. no. 2105016, doi: 10.1002/advs.202105016.
5. Y. Wang, W. Zhang, C. Liu, J. Sun, and C.-X. Wang, ''Reconfigurable intelligent surface for NLOS integrated sensing and communications,'' in Proc. IEEE/CIC Int. Conf. Commun. China (ICCC), IEEE, Aug. 2022,pp. 708–712, doi: 10.1109/ICCC55456.2022.9880639.
6. B. C. Mabuza and S. Sinha, ''The tunnelling and electron injection reliabilities for FG transistors,'' Microelectron. Int., vol. 31, no. 2, pp. 108–115, Apr. 2014, doi: 10.1108/mi-01-2013-0001.
7. J. T. Valliarampath and S. Sinha, ''Designing linear PAs at millimeter-wave frequencies using Volterra series analysis,'' Can. J. Electr. Comput. Eng., vol. 38, no. 3, pp. 232–237, Summer 2015. W. Lambrechts, S. Sinha, and S. Mosoetsa, ''Colonization by algo- rithms in the fourth industrial revolution,'' IEEE Access, vol. 10, pp. 11057–11064, 2022, doi: 10.1109/ACCESS.2022.3145236.
8. F. Wang, S. Xu, J. Romberg, and H. Wang, ''An artificial-intelligence (AI) assisted mm-wave Doherty power amplifier with rapid mixed-mode in- field performance optimization,'' in IEEE MTT-S Int. Microw. Symp. Dig., Aug. 2019, pp. 1–3, doi: 10.1109/IMC-5G47857.2019.9160368.
9. H. Yu, H. Chalamalasetty, and M. Swaminathan, ''Modeling of voltage-controlled oscillators including I/O behavior using augmented neural networks,'' IEEE Access, vol. 7, pp. 38973–38982, 2019, doi: 10.1109/ACCESS.2019.2905136.
10. R. Braithwaite, ''A self-generating coefficient list for machine learning in RF power amplifiers using adaptive predistortion,'' in Proc. Eur. Microw. Conf., Sep. 2006, pp. 1229–1232, doi: 10.1109/EUMC.2006.281199.
11. E. Afacan, N. Lourenço, R. Martins, and G. Dündar, ''Review: Machine learning techniques in analog/RF integrated circuit design, synthesis, layout, and test,'' Integration, vol. 77, pp. 113–130, Mar. 2021, doi: 10.1016/j.vlsi.2020.11.006.
12. G. E. Moore, ''Cramming more components onto integrated circuits, reprinted from electronics, volume 38, number 8, April 19, 1965, pp. 114 ff,'' IEEE Solid-State Circuits Soc. Newslett., vol. 11, no. 3, pp. 33–35, Sep. 2006, doi: 10.1109/n-ssc.2006.4785860.
13. S. Sinha and K. Sengupta, ''Examining the impact of 6G telecommunications on society what to consider before the next generation of connectivity,'' IEEE Spectr, Jan. 2023. [Online]. Available: https:// spectrum.ieee.org/examining-the-impact-of-6g-telecommunications-on- society
14. M. Bozanic and S. Sinha, Mobile Communication Networks: 5G and a Vision of 6G, vol. 751. Cham, Switzerland: Springer, 2021, doi: 10.1007/978-3-030-69273-5.
15. A. Bimana and S. Sinha, ''Highly sensitive broadband SiGe HBT LNA: Genetic algorithm based optimization and design methodology,'' in Proc. IEEE 41st Int. Conf. Electron. Nanotechnol. (ELNANO), Oct. 2022, pp. 701–706, doi: 10.1109/ELNANO54667.2022.9927081.
16. Q.-J. Zhang, K. C. Gupta, and V. K. Devabhaktuni, ''Artificial neural networks for RF and microwave design-from theory to practice,'' IEEE Trans. Microw. Theory Techn., vol. 51, no. 4, pp. 1339–1350, Apr. 2003, doi: 10.1109/TMTT.2003.809179.
17. A. Suissa, O. Romain, J. Denoulet, K. Hachicha, and P. Garda, ''Empirical method based on neural networks for analog power modeling,'' IEEE Trans. Comput.-Aided Design Integr. Circuits Syst., vol. 29, no. 5, pp. 839–844, May 2010, doi: 10.1109/TCAD.2010.2043759.

18. M. Grabmann, F. Feldhoff, and G. Gläser, ‘‘Power to the model: Generating energy-aware mixed-signal models using machine learning,’’ in Proc. 16th Int. Conf. Synth., Model., Anal. Simul. Methods Appl. Circuit Design (SMACD), Jul. 2019, pp. 5–8, doi: 10.1109/SMACD.2019.8795295.
19. V. Ceperic and A. Baric, ‘‘Modeling of analog circuits by using support vector regression machines,’’ in Proc. 11th IEEE Int. Conf. Electron., Cir- cuits Syst., Dec. 2004, pp. 391–394, doi: 10.1109/ICECS.2004.1399700.
20. M. Ding and R. I. Vemur, ‘‘An active learning scheme using support vector machines for analog circuit feasibility classification,’’ in Proc. 18th Int. Conf. VLSI Design Held Jointly, 4th Int. Conf. Embedded Syst. Design, Jan. 2005, pp. 528–534, doi: 10.1109/ICVD.2005.47.
21. L. Safatly, M. Bkassiny, M. Al-Husseini, and A. El-Hajj, ‘‘Cognitive radio transceivers: RF, spectrum sensing, and learning algorithms review,’’ Int. J. Antennas Propag., vol. 2014, pp. 1–21, 2014, doi: 10.1155/2014/548473.
22. A. Muduli and K. Panwar, ‘‘A reconfigurable filtenna for cognitive radio application,’’ J. Phys., Conf., vol. 1817, no. 1, Mar. 2021, Art. no. 012002, doi: 10.1088/1742-6596/1817/1/012002.
23. H. Lalj, H. Griguer, and M. Drissi, ‘‘Design of reconfigurable band notches antenna for cognitive radio applications,’’ Wireless Eng. Technol., vol. 5, no. 3, pp. 99–105, 2014, doi: 10.4236/wet.2014.53011.
24. A. A. Ibrahim, W. A. E. Ali, M. Alathbah, and H. A. Mohamed, ‘‘A frequency reconfigurable folded antenna for cognitive radio com- munication,’’ Micromachines, vol. 14, no. 3, p. 527, Feb. 2023, doi: 10.3390/mi14030527.
25. L. Zhang, B. Chi, N. Qi, L. Liu, H. Jiang, and Z. Wang, ‘‘A lower power reconfigurable multi-band transceiver for short-range communi- cation,’’ J. Semicond., vol. 34, no. 3, Mar. 2013, Art. no. 035008, doi: 10.1088/1674-4926/34/3/035008.
26. O. Chatterjee, ‘‘Design and implementation of reconfigurable modulator using FPGA for cognitive radio system,’’ HELIX, vol. 8, no. 6, pp. 4418–4425, Oct. 2018, doi: 10.29042/2018-4418-4425.
27. P. Xu, Z. Zhu, H. Chu, and M. Li, ‘‘Channel estimation for reconfigurable intelligent surface-assisted multiple antennas communication systems,’’ in Proc. Int. Conf. Eng. Educ. Inf. Technol. (EEIT), May 2022, pp. 88–92, doi: 10.1109/EEIT56566.2022.00028.
28. A. Borel, V. Barzdenas, and A. Vasjanov, ‘‘Linearization as a solution for power amplifier imperfections: A review of methods,’’ Electronics, vol. 10, no. 9, p. 1073, May 2021, doi: 10.3390/electronics10091073.
29. C. Baylis, R. J. Marks, A. Egbert, and C. Latham, ‘‘Artificially intelligent power amplifier array (AIPAA): A new paradigm in reconfigurable radar transmission,’’ in Proc. IEEE Radar Conf., May 2021, pp. 1–5, doi: 10.1109/RadarConf2147009.2021.9455195.
30. C. R. Chappidi and K. Sengupta, ‘‘A 26–42 GHz broadband, back-off efficient and vswr tolerant CMOS power amplifier architecture for 5G applications,’’ in Proc. Symp. VLSI Circuits, Jun. 2019, pp. 22–23, doi: 10.23919/VLSIC.2019.8778095.
31. Y. Yu, P. Chen, X.-W. Zhu, J. Zhai, and C. Yu, ‘‘Continual learning digital predistortion of RF power amplifier for 6G AI-empowered wireless communication,’’ IEEE Trans. Microw. Theory Techn., vol. 70, no. 11, pp. 4916–4927, Nov. 2022, doi: 10.1109/TMTT.2022.3210199.
32. K. Datta and H. Hashemi, ‘‘Watt-level mm-wave power amplification with dynamic load modulation in a SiGe HBT digital power amplifier,’’ IEEE J. Solid-State Circuits, vol. 52, no. 2, pp. 371–388, Feb. 2017, doi: 10.1109/JSSC.2016.2622710.
33. T. Zimmer, J. Bock, F. Buchali, P. Chevalier, M. Collisi, B. Debaillie, M. Deng, P. Ferrari, S. Fregonese, C. Gaquiere, and H. Ghanem, ‘‘SiGe HBTs and BiCMOS technology for present and future millimeter-wave

systems,'' IEEE J. Microw., vol. 1, no. 1, pp. 288–298, Jan. 2021, doi: 10.1109/JMW.2020.3031831.
34. R. Guo, K. Qian, J. Wei, T. Chen, Y. Liu, D. Kong, J. J. Wang, Y. Wu, S. G. Hu, Q. Yu, and Y. Liu, ''Design of a neural network-based VCO with high linearity and wide tuning range,'' IEEE Access, vol. 7, pp. 60120–60125, 2019, doi: 10.1109/ACCESS.2019.2915335.
35. N. Kandpal, A. Singh, and A. Agarwal, ''A machine learning driven PVT-robust VCO with enhanced linearity range,'' Circuits, Syst., Signal Process., vol. 41, no. 8, pp. 4275–4292, Aug. 2022, doi: 10.1007/s00034- 022-02001-x.
36. E. Kuprikov, A. Perepelov, A. Kokhanovskiy, I. A. Bednyakova, and S. Turitysin, ''Designing mamyshev oscillator cavity by particle swarm optimization algorithm,'' in Proc. Int. Conf. Laser Opt. (ICLO), Jun. 2022, Paper R2-p29, doi: 10.1109/ICLO54117.2022.9840077.
37. A. Zhang and J. Gao, ''InP HBT small signal modeling based on artificial neural network for millimeter-wave application,'' in IEEE MTT-S Int. Microw. Symp. Dig., Dec. 2020, pp. 1–3, doi: 10.1109/NEMO49486.2020.9343502.
38. P. Sen, W. H. Woods, S. Sarkar, R. J. Pratap, B. M. Dufrene, R. Mukhopadhyay, C.-H. Lee, E. F. Mina, and J. Laskar, ''Neural- network-based parasitic modeling and extraction verification for RF/millimeter-wave integrated circuit design,'' IEEE Trans. Microw. Theory Techn., vol. 54, no. 6, pp. 2604–2614, Jun. 2006, doi: 10.1109/TMTT.2006.872926.
39. L. E. Frenzel, ''Radio/wireless,'' in Electronics Explained. Amsterdam, The Netherlands: Elsevier, 2018, pp. 159–194, doi: 10.1016/B978-0-12- 811641-8.00007-2.
40. J. Luomala and I. Hakala, ''Effects of temperature and humidity on radio signal strength in outdoor wireless sensor networks,'' in Proc. Federated Conf. Comput. Sci. Inf. Syst., Oct. 2015, pp. 1247–1255, doi: 10.15439/2015F241.
41. W. Xiao, Z. Luo, and Q. Hu, ''A review of research on signal modulation recognition based on deep learning,'' Electronics, vol. 11, no. 17, p. 2764, Sep. 2022, doi: 10.3390/electronics11172764.
42. Z. Fu, X. Zou, Y. Liao, G. Lai, Y. Li, and K. L. Chung, ''A brief review and comparison between transmitarray antennas, reflectarray antennas and reconfigurable intelligent surfaces,'' in Proc. IEEE Conf. Telecommun., Opt. Comput. Sci. (TOCS), Dec. 2022, pp. 1192–1196, doi: 10.1109/TOCS56154.2022.10016145.
43. H. Jadhav, V. B. Kumaravelu, F. R. C. Soria, M. S. Sayeed, and A. Murugadass, ''Smart reconfigurable intelligent surface with discrete phase shifter for next generation networks,'' in Proc. Int. Conf. Wireless Commun. Signal Process. Netw. (WiSPNET), Mar. 2022, pp. 178–182, doi: 10.1109/WiSPNET54241.2022.9767157.
44. S. H. Zainud-Deen, ''Reconfigurable intelligent surfaces for wireless communications,'' in Proc. 39th Nat. Radio Sci. Conf. (NRSC), vol. 1, Nov. 2022, p. 342, doi: 10.1109/NRSC57219.2022.9971201. K. Wang, C.-T. Lam, and B. K. Ng, ''Doppler effect mitigation using reconfigurable intelligent surfaces with hardware impairments,'' in Proc. IEEE Globecom Workshops (GC Wkshps), Dec. 2021, pp. 1–6, doi: 10.1109/GCWkshps52748.2021.9681939.
45. J. V. Alegria and F. Rusek, ''Channel orthogonalization with reconfigurable surfaces,'' in Proc. IEEE Globecom Workshops (GC Wkshps), Dec. 2022, pp. 37–42, doi: 10.1109/GCWkshps56602.2022.10008751.
46. P. Tulupov, B. Sorokin, and A. Korolev, ''Coverage impact of reconfig- urable intelligent surfaces in 6G mobile networks,'' in Proc. Int. Conf. Electr., Comput. Energy Technol. (ICECET), Jul. 2022, pp. 1–5, doi: 10.1109/ICECET55527.2022.9872978.
47. T. Oliveira and W. A. M. Van Noije, ''Design of analog integrated circuits using simulated

annealing/quenching with crossovers and particle swarm optimization,'' in Simulated Annealing—Advances, Applications and Hybridizations. London, U.K.: InTech, 2012, doi: 10.5772/50384.

48. S. Er, E. Liu, M. Chen, Y. Li, Y. Liu, T. Zhao, and H. Wang, ''Deep learning assisted end-to-end synthesis of mm-wave passive networks with 3D EM structures: A study on a transformer-based matching network,'' in IEEE MTT-S Int. Microw. Symp. Dig., Jun. 2021, pp. 66–69.
49. B. Liu, D. Zhao, P. Reynaert, and G. G. E. Gielen, ''Synthesis of integrated passive components for high-frequency RF ICs based on evolutionary computation and machine learning techniques,'' IEEE Trans. Comput.- Aided Design Integr. Circuits Syst., vol. 30, no. 10, pp. 1458–1468, Oct. 2011, doi: 10.1109/TCAD.2011.2162067.
50. E. Ali Karahan, Z. Liu, and K. Sengupta, ''Deep-Learning-Based inverse- designed millimeter-wave passives and power amplifiers,'' IEEE J. Solid-State Circuits, vol. 58, no. 11, pp. 3074–3088, Nov. 2023, doi: 10.1109/JSSC.2023.3276315.
51. H. M. El Misilmani and T. Naous, ''Machine learning in antenna design: An overview on machine learning concept and algorithms,'' in Proc. Int. Conf. High Perform. Comput. Simulat. (HPCS), Jul. 2019, pp. 600–607, doi: 10.1109/HPCS48598.2019.9188224.
52. J. R. Koza, F. H. Bennett, III, D. Andre, and M. A. Keane, ''Synthesis of topology and sizing of analog electrical circuits by means of genetic programming,'' Comput. Methods Appl. Mech. Eng., vol. 186, nos. 2–4, pp. 459–482, Jun. 2000, doi: 10.1016/S0045-7825(99)00397-7.
53. Y. Jiang, J. Ju, X. Zhang, and B. Yang, ''Automated analog cir- cuit design using genetic algorithms,'' in Proc. 3rd Int. Conf. Anti- Counterfeiting, Secur., Identificat. Commun., Aug. 2009, pp. 223–228, doi: 10.1109/ICASID.2009.5276912.
54. J. D. Lohn, G. L. Haith, S. P. Colombano, and D. Stassinopoulos, ''Towards evolving electronic circuits for autonomous space applica- tions,'' in Proc. IEEE Aerospace Conf., Mar. 2000, pp. 473–486, doi: 10.1109/AERO.2000.878523.
55. X. Yan, W. Li, Y. Zhang, H. Zhang, and J. Wu, ''Electronic circuit automatic design based on genetic algorithms,'' Proc. Eng., vol. 15, pp. 2948–2954, Jan. 2011, doi: 10.1016/j.proeng.2011.08.555.
56. C. Mattiussi, ''Evolutionary synthesis of analog networks,'' IEM, Lau- sanne, Switzerland, Tech. Rep. 3199, 2005.
57. C. Mattiussi and D. Floreano, ''Analog genetic encoding for the evolution of circuits and networks,'' IEEE Trans. Evol. Comput., vol. 11, no. 5, pp. 596–607, Oct. 2007, doi: 10.1109/TEVC.2006.886801.
58. G. R. Salgado and C. A. Reyes-Garcia, ''Applications of evolutionary algorithms in the design automation of analog integrated circuits,'' J. Appl. Sci., vol. 10, no. 17, pp. 1859–1872, Aug. 2010, doi: 10.3923/jas.2010.1859.1872.
59. C. H. Oxley and M. J. Uren, ''Measurements of unity gain cutoff frequency and saturation velocity of a GaN HEMT transistor,'' IEEE Trans. Electron Devices, vol. 52, no. 2, pp. 165–169, Feb. 2005, doi: 10.1109/TED.2004.842719.
60. B. Heinemann, H. Rucker, R. Barth, F. Bärwolf, J. Drews, G. G. Fischer, A. Fox, O. Fursenko, T. Grabolla, F. Herzel, and J. Katzer, ''SiGe HBT with fx/fmax of 505 GHz/720 GHz,'' in IEDM Tech. Dig., Dec. 2016, pp. 1–4, doi: 10.1109/IEDM.2016.7838335.
61. J.-S. Yoon and R.-H. Baek, ''Device design guideline of 5-nm-node FinFETs and nanosheet FETs for analog/RF applications,'' IEEE Access, vol. 8, pp. 189395–189403, 2020, doi: 10.1109/ACCESS.2020.3031870.
62. W. Hafez, J.-W. Lai, and M. Feng, ''InP/InGaAs SHBTs with 75 nm collector and fT>500 GHz,'' Electron.

Lett., vol. 39, no. 20, p. 1475, 2003, doi: 10.1049/el:20030951.
63. R. Lovblom, R. Fluckiger, M. Alexandrova, O. Ostinelli, and C. R. Bolognesi, ‘‘InP/GaAsSb DHBTs with simultaneous f T/f MAX = 428/621 GHz,’’ IEEE Electron Device Lett., vol. 34, no. 8, pp. 984–986, Aug. 2013, doi: 10.1109/LED.2013.2269711.
64. S. Hashima, Z. M. Fadlullah, M. M. Fouda, E. M. Mohamed, K. Hatano, B.M. ElHalawany, and M. Guizani, ‘‘On softwarization of intelligence in 6G networks for ultra-fast optimal policy selection: Challenges and opportunities,’’ IEEE Netw., vol. 37, no. 2, pp. 190–197, Mar./Apr. 2023, doi: 10.1109/MNET.103.2100587.
65. A. J. Pazhani. A, P. Gunasekaran, V. Shanmuganathan, S. Lim, K. Madasamy, R. Manoharan, and A. Verma, ‘‘Peer–peer communication using novel slice handover algorithm for 5G wireless networks,’’ J. Sensor Actuator Netw., vol. 11, no. 4, p. 82, Nov. 2022, doi: 10.3390/jsan11040082.
66. C. de Alwis, Q. Pham, and M. Liyanage, 6G Frontiers. Hoboken, NJ, USA: Wiley, 2022, doi: 10.1002/9781119862321.
67. Z. Liu, E. A. Karahan, and K. Sengupta, ‘‘Deep learning-enabled inverse design of 30–94 GHz psat,3dB SiGe PA supporting concurrent multiband operation at multi-Gb/s,’’ IEEE Microw. Wireless Compon. Lett., vol. 32, no. 6, pp. 724–727, Jun. 2022, doi: 10.1109/LMWC.2022.3161979.
68. M. C. Wanke, M. Lee, C. D. Nordquist, M. J. Cich, M. Cavaliere, A. M. Rowen, J. R. Gillen, C. L. Arrington, A. D. Grine, C. T. Fuller, and J. L. Reno, ‘‘Integrated chip-scale THz technology,’’ Proc. SPIE, vol. 8031, May 2011, Art. no. 80310E, doi: 10.1117/12.883612.
69. X. Wu and K. Sengupta, ‘‘Dynamic waveform shaping for reconfigurable radiated periodic signal generation with picosecond time-widths,’’ in Proc. IEEE Custom Integr. Circuits Conf. (CICC), Sep. 2015, pp. 1–4, doi: 10.1109/CICC.2015.7338411.
70. K. Sengupta and A. Hajimiri, ‘‘Distributed active radiation for THz signal generation,’’ in Proc. IEEE Int. Solid-State Circuits Conf., Feb. 2011, pp. 288–289, doi: 10.1109/ISSCC.2011.5746322.
71. K. Sengupta, T. Nagatsuma, and D. M. Mittleman, ‘‘Terahertz integrated electronic and hybrid electronic-photonic systems,’’ Nature Electron., vol. 1, no. 12, pp. 622–635, Dec. 2018, doi: 10.1038/s41928-018-0173-2.
72. K. Sengupta, ‘‘Lecture by Dr. Kaushik Sengupta (IEEE SSCS DL; IEEE MTT-S DML (2021–23)),’’ Tech. Rep., Dec. 2020. [Online]. Available: https://www.youtube.com/watch?v=QjU-jI6v9GE
73. K. Sengupta and A. Hajimiri, ‘‘A 0.28 THz power-generation and beam- steering array in CMOS based on distributed active radiators,’’ IEEE J. Solid-State Circuits, vol. 47, no. 12, pp. 3013–3031, Dec. 2012, **doi:** 10.1109/JSSC.2012.2217831.