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# Soft-Error Reduction and Enhancement of Write Stability and Hold Power Optimization by using 12T SRAM For Aerospace Applications

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**Abstract**
As the technology has rapidly evolved and also high-speed task implementation has come into picture the chance for an error to occur has also increased though there are many precision algorithms to increase the precision of the system significantly this paper proposes one such error reducing application for aerospace applications. Using a Quadruple Cross-Coupled Latch-Based 10T and 12T SRAM Bit-Cell Designs for Highly Reliable Terrestrial Applications (QUCCE12T) is more susceptible to data loss as the QUCCE12T SRAM has high sensitivity and the sensitive nodes are at higher risk. To reduce this, we propose to use Soft-Error Reduction and Enhancement of Write Stability and Hold Power Optimization by using 12T SRAM (SREWH12T). Basically, the initial thought is to reduce the soft error created by voltage drops by passing the data through the inverters. The Single Event Upset (SEU) that arise in the usage of QUCCE12T SRAM can be recovered using a SREWH12T SRAM instead. The sensitive components of SREWH12T have the capability to recover their data even in cases where the values have been altered by radiation impact. The SREWH12T SRAM cell to mitigate upsets, compares it with other cells, and demonstrates its superior performance in terms of soft-error tolerance, recovery from upsets and having low power consumption. Furthermore, the added advantage of SREWH12T cell is that it can recover from Single Event Multiple Nodes Upset (SEMNU). Average power consumed by SREWH12T is 2.988363e-007 watts. Along with this the SREWH12T SRAM can provide high write stability due to its recovery rate. All these added advantages and recovery of data all comes at high utility range and with slightly high read energy consumption, which is very minimal, the system also exhibits slightly high read delay.

**Keywords:** Single-Event Upset (SEU), Single-Event Multimode Upsets (Semnus), Critical Charge, Radiation Hardness, Write Stability, Hold Power.

## I. Introduction

The aerospace sector has significantly simplified human life and bolstered security through various utilities such as satellite communications, military surveillance, guidance, and tracking systems.

Microprocessors find extensive application in aerospace for functions like control, guidance, engine control, and inertial navigation, often integrating multiple cores to enhance performance. This increase in core count necessitates a higher cache memory capacity, making SRAM cells crucial for power, area, and delay optimization of processors. The deep space environment harbors highly energetic particles that can disrupt the operation of memory circuits. When these particles collide with the substrate of an integrated circuit, they generate electron-hole pairs, leading to the creation of voltage spikes that, if surpassing the logic circuit's switching threshold and enduring for sufficient durations, may induce a single-event upset (SEU) or soft error. Moreover, Because of intense advancements in technology scaling, reduced spacing between integrated circuit devices increases the likelihood of a single ion strike affecting multiple nodes, potentially leading to a single-event multi-node upset (SEMNU). The SREWH12T cell boasts the following noteworthy features:

1. Immunity to single-event upsets (SEUs) of both polarities at any sensitive node.
2. Capability to recover from single-event multi-node upsets (SEMNUs) occurring at its storage node-pair.
3. Minimal hold power consumption compared to the considered cells.
4. Improved read stability, wherein the '0'-storing storage node, accessed directly by the bit line during read operations, can recover from any disruption.
5. Enhanced write ability and reduced write delay compared to most of the cells under comparison.
6. The subsequent sections of this paper are structured as follows: Section II elucidates the fundamental operations and SEU recovery capabilities of the proposed SREWH12T cell. The simulation setup and comparative analysis are detailed in Section III. Finally, Section IV provides the concluding remarks of this study.

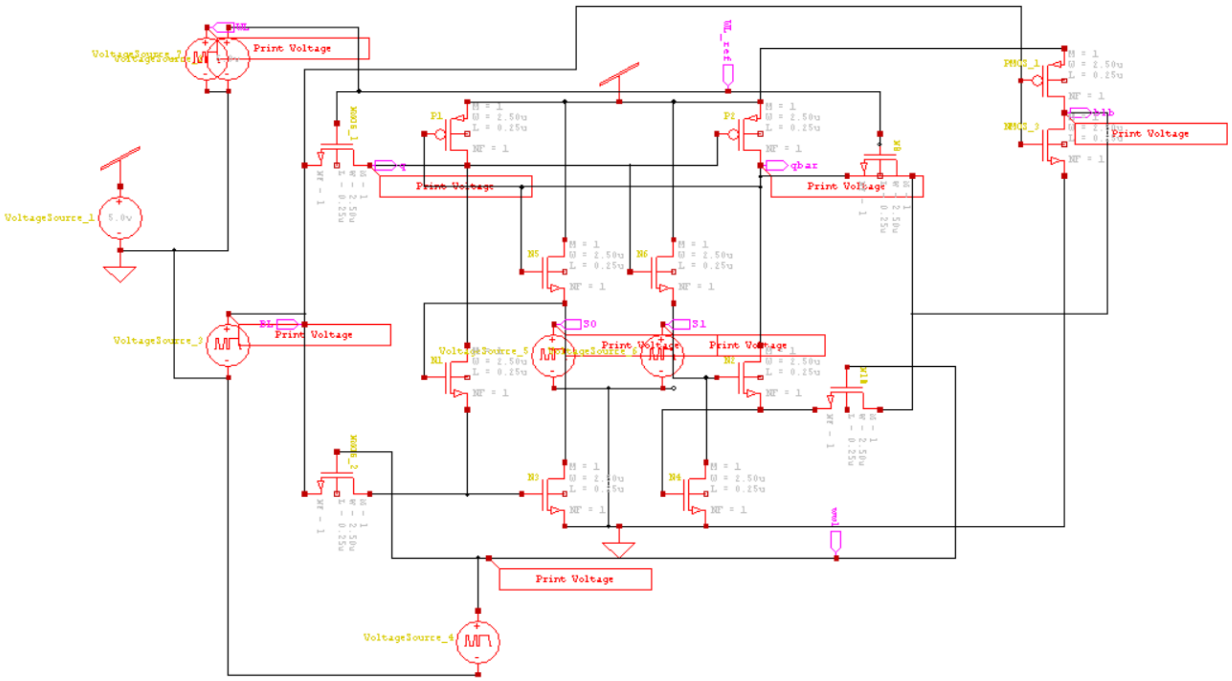



**Figure 1: Schematic of the SREWH12T SRAM cell.**

## II. Literature Survey

The literature survey in Ch Santhi Rani, D Sudha, Sreenivasa Rao Ijjada [3] comparing the proposed 10T SRAM cell design in both CMOS and Fin FET technologies with existing cell designs in the literature to showcase its advantages in terms of stability and power consumption.Wing-Hung Ki and Chi-Ying Tsui [1] SARP12T is immune to SEUs of both polarities induced at any sensitive node and can recover from SEMNUs that occur at its storage node-pair also consumes the lowest hold power dominance among all the cells under consideration. Ch Santhi Rani, D Sudha, Sreenivasa Rao [2] summarizes the importance of semiconductor memories, the challenges in bulk CMOS scaling, and the advantages of using Fin FET technology as an alternative. Ji Sang Oh and Juhyun Park [7] discusses the challenges faced by conventional SRAM bitcells in the near-V region with a bit-interleaved structure and the proposed solutions to address these challenges, including the differential 7T SRAM bit cell with an additional PMR NMOS transistor.Jae-Won Nam, Ju-Hyeok Ahn [6] discusses the need for advanced security systems for IoT devices, introduces PUFs as a solution, explains different types of PUFs, and highlights the advantages of memory-based PUFs. It also mentions the potential application of a proposed technique to reduce transistors in PUF structures., Daisuke Kobayashi, Kauyuki Hirose [11] Examining six cases of SRAMs in different technology nodes and processes, collecting cross section curves and model parameters from various sources in the literature. Chunyu Peng, Jiati Huang [13] discusses the challenges of soft errors in SRAM, various alternative SRAM cell designs to improve radiation hardness, and introduces the novel radiation-hardened RSP-14T SRAM cell with improved performance metrics and also emphasizes the importance of layout-level optimization and TCAD mixed-mode simulations in evaluating the SEU immunity and rephrase the tolerance of the suggested plan. The literature survey in M Pown, B Lakshmi [8] includes mitigation techniques for SEU effects in specific circuit designs, and an in-depth analysis of soft error performance, mitigation techniques, and power consumption in a specific SRAM cell using DG TFETs. Alok Kumar Shukla, Seema Dhull [12] discusses the challenges of SEUs and DNUs in VLSI circuits, the emergence of hybrid spintronic/CMOS technology. Soumitrapal, Gajendranath chowdary [9] includes a comparison of various soft-error-aware SRAM cells proposed in different papers, highlighting their strengths and weaknesses in terms of SEU recovery, read stability, hold power consumption, write ability, and overall performance metrics. Azam Seyedi [14] includes a review of previously proposed design solutions for robustness in memory designs, highlighting the Quatro cell, PMOS stacked (PS) and NMOS stacked (NS) cells, a 12T radiation-hardened memory cell. radiation hardened memory cell, and the Gain Cell eDRAM (GC-eDRAM).Govind Prasad, Chandra Mandi, Maifuz Ali, B C Mandi [10] discusses the challenges faced by existing SRAM cells, introduces the 10T SRAM cell as a solution, and presents the proposed RHBD SRAM cell as offering better soft error resilience, Offering superior noise tolerance, reduced power usage, smaller footprint, and similar speed compared to alternative cell designs. Yuri Hong, Yejoo Choi [5] includes discussions on the use of NCFET for lower power applications, the potential improvement in read/write performance compared to conventional SRAM, the introduction of the cell sigma concept for yield estimation, and the comparison of sensitivities in NCFET-based SRAM and baseline SRAM.

## III. THE PROPOSED SREWH14T CELL AND ITS OPERATION

SREWH12T comprises two-word lines, WL and WWL, along with two storage nodes, Q and QB, and two internal nodes, S1 and S0. WL governs the access transistors N7 and N8, facilitating the connection of storage nodes Q and QB with their respective bit lines BL and BLB. The internal nodes S1 and S0 are

linked to their corresponding bit lines BL and BLB via access transistors N9 and N10, controlled by WWL. When considering SREWH12T and all comparison cells storing '1', wherein Q = '1' and QB = '0', the internal nodes S1 and S0 store '1' and '0', respectively.

**A. Basic Operations**

All fundamental operations of the SREWH12T SRAM cell as follows:

1. **Hold Operation:** During the hold mode, both sets of access transistors are deactivated by pulling down both WL and WWL to the ground (GND). To minimize read delay, bit lines are pre charged to the voltage supply (VDD) during this mode. Consequently, during the hold state, transistors P1, N2, N3, and N6 are switched on, while the remaining transistors are off for the considered scenario. This configuration ensures that SREWH14T maintains its initial stored data (refer to Fig. 3).
2. **Write Operation:** The write operation is initiated by activating both word lines (WL and WWL), thereby turning on both sets of access transistors (N7/N8 and N9/N10). As BL is grounded, nodes Q and S1 are pulled down by BL through transistors N7 and N9, respectively. The cross-coupling between transistor P1 and transistor P2 amplifies the potential difference between nodes Q and QB, facilitating a successful write operation.
3. **Read Operation:** During the read operation, WL is connected to VDD while WWL remains inactive. Consequently, access transistors N7 and N8 are activated, while access transistors N9 and N10 are deactivated. Bit lines are pre charged to VDD for read operations. The voltage difference between BL and BLB reaching 50 mV, a sense amplifier (not depicted) senses the stored data, completing the read operation.

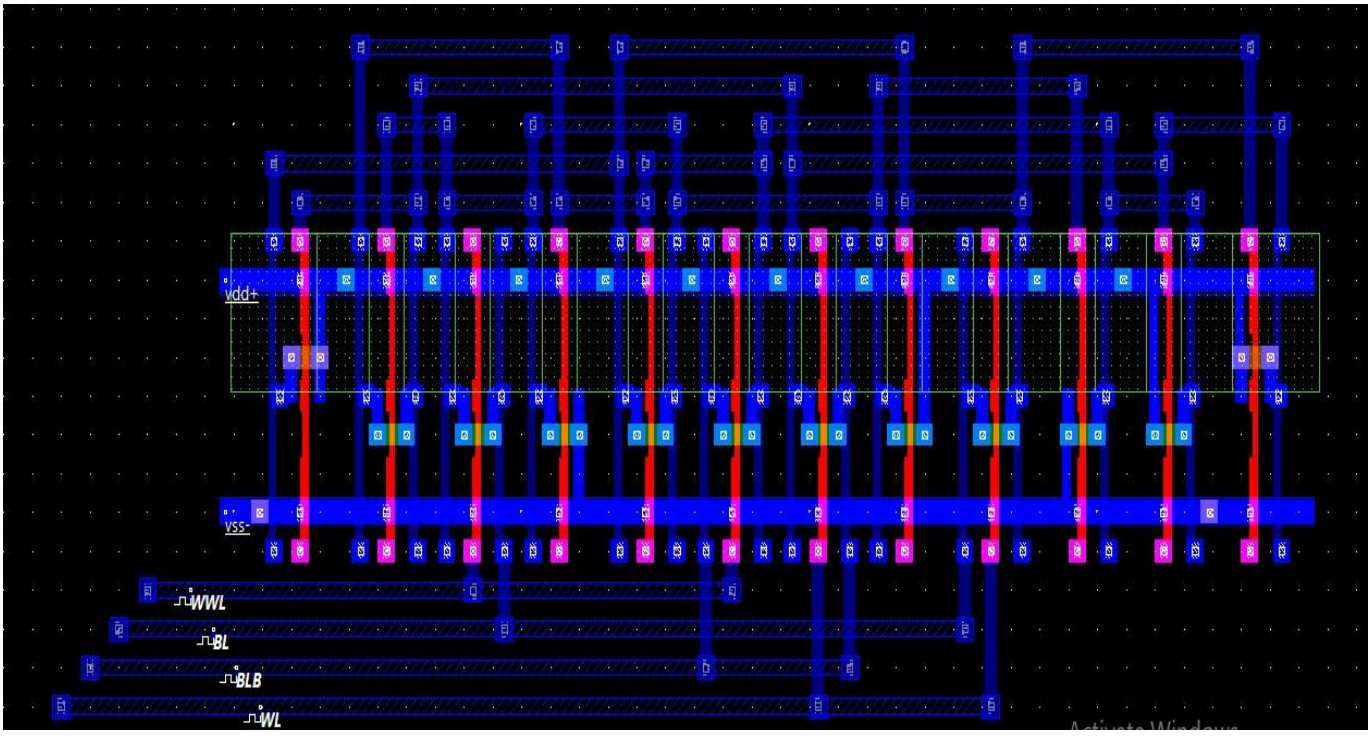



**Figure 2: Thin cell Layout of SREWH12T SRAM cell.**

**B. SEU Recovery Analysis**

The response of the proposed cell to a single-event upset (SEU), elucidating the distinctive transient pulses induced by radiation particles striking the drain terminals of PMOS and NMOS transistors. Specifically,

it articulates how such occurrences manifest as '0' to '1' or '1' to '1' pulses in PMOS transistors and '0' to '0' or '1' to '0' pulses in NMOS transistors. Additionally, it highlights the insensitivity of node S0 due to its strategic placement amidst the drain terminals of NMOS transistors, thus underscoring its resilience against SEUs.

1. **SEU @ S1:** When the '1'-storing internal node S1 experiences an SEU, transitioning from '1' to '0', transistors N2 and N3 are deactivated. However, pull-up transistor P2 corresponding to QB remains inactive due to the unaffected node Q. Consequently, with both pull-up and pull-down paths disconnected for QB, it enters a high-impedance state, maintaining its initial logic value and keeping transistor N5 inactive. Thus, node S0 also enters a high-impedance state, retaining its original logic value. Given the unchanged states of Q, QB, and S0, S1 eventually restores the which its haves initially.
2. **SEU @ Q:** In the event of an SEU affecting the '1'-storing storage node Q, transitioning its logic state to '0', transistors P2 and N6 are momentarily activated and deactivated, respectively. With N6 and N4 (maintained inactive in hold mode) both off, node S1 enters a high-impedance state and preserves its logic value. Consequently, N2 remains active, ensuring Q retrieves its initial data.

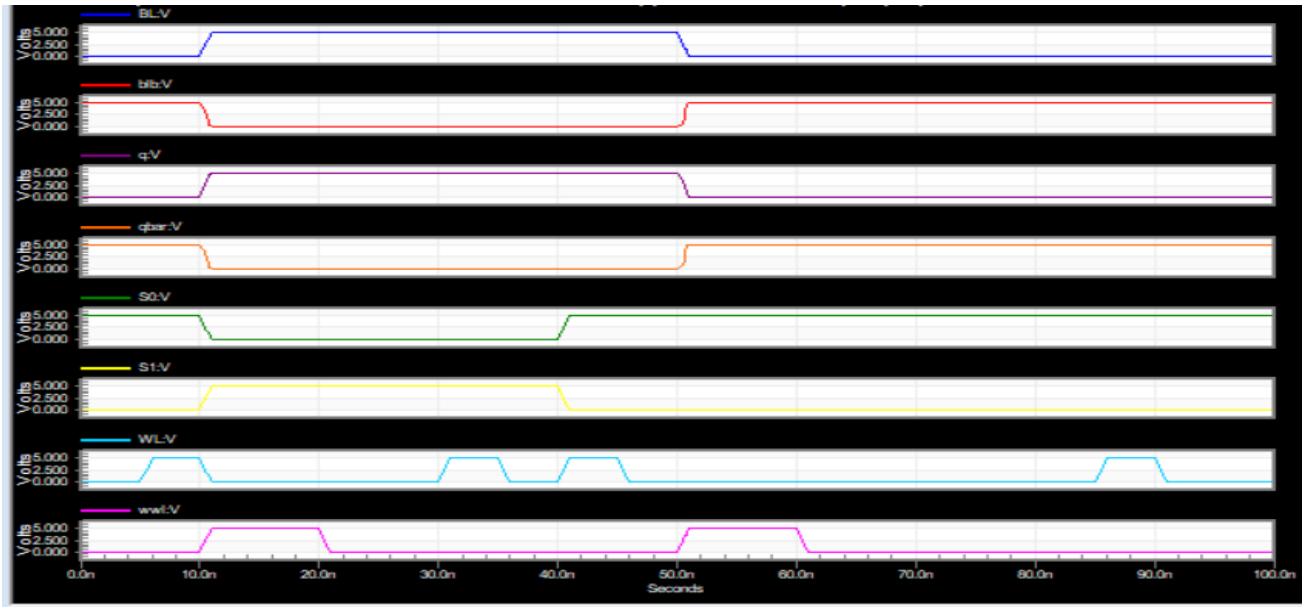



**Figure 3: Soft-error recovery at different nodes of the SREWH12T SRAM cell.**

3. **SEU @ QB:** When a strong SEU affects the QB storage node, changing it from '0' to '1' as shown in Fig. 3, it causes some changes in the circuit. Specifically, P1 turns off temporarily while N5 turns on temporarily. Even though N5 turns on, S0's state stays the same because N3, which stays on due to its hold mode, is bigger than N5As a result, QB discharges to the ground, shown in Fig. 3.
4. **SEMNU @ Q-QB**: The new SREWH12T cell can handle SEU effects at S1, Q, or QB, and SEMNU at the Q-QB pair. However, if too much charge builds up at S1-Q/S1-QB, S1 might switch, causing data change. To avoid this, keep N type metal oxide semiconductor and P type metal oxide semiconductor transistors apart by more than 2 μm (0.6 μm).

## IV. SIMULATION SETUP AND RESULTS

### A. Read Delay Comparison

The read delay, also known as access time (TRA), is assessed as the duration needed to establish a 50-mV voltage disparity between the bit lines once WL referred as the word line surpasses 50% during its rising

edge. Thus, the cell ratio (CR) plays a pivotal role in facilitating the comparison of read delays. As exemplified in Figure 4, a shorter TRA compared to QUCCE12T (CR = 2.5) owing to its higher CR value.

**B. Read Static Noise Margin Comparison**

The proposed SREWH12T showcases a slightly lower RSNM at very low voltages, it demonstrates a higher RSNM at higher voltages. This phenomenon arises because the '0'-storing storage node QB of SREWH12T, during read operation, the bit line directly accesses can able to recover from any upset (as elucidated in Section III-B.3) at higher voltages.

**C. Write Delay and Write Ability Comparison**

The measure of write delay, also known as access time (TWA), is determined by the time difference between the point at which the WL reaches 50% of its maximum swing and the activation of the storage nodes Q and QB intersect each other. This disparity arises because the pull-up path associated with its initially '1'-storing internal node weakens as the voltage at QB.

**D. Energy Consumption Analysis**

Static Random Access Memory cell, dynamic power is partitioned into two distinct components: read power and write power. Consequently, the power consumption during write operations significantly exceeds that during read operations. Traditional SRAM cells experience increased power usage primarily due to the frequent discharge operations on their bit lines. The notable reduction in commendable efficacy of power management within the suggested SRAM can be credited to its adept strategy in minimizing power consumption within the SRAM cells. Thus, it is crucial to assess the energy consumption per read/write cycle for all comparison cells.

1. **Read Energy Consumption:** The energy consumption during read operations (EREAD) of various cells under different VDD conditions is depicted in Figure 8. Cell, QUCCE12T, which feature a single access transistor adjacent to each bit line, exhibit lower bit line capacitance, resulting in reduced dynamic power consumption.
2. **Write Energy Consumption:** Energy consumption during write operations of cells under different VDD conditions, as depicted in Figure 9. Particularly praiseworthy is the acknowledgment that SREWH12T cells demonstrate lower EWRITE, attributed to their notably reduced dynamic power consumption.

**E. Hold Power Comparison**

Power dissipation, particularly due to bit line leakage and leakage in inverters, constitutes a notable portion of the overall power consumption in an SRAM cell. Figure 10 illustrates a comparison of the power dissipation for all cells under consideration. It is evident that the QUCCE12T cell exhibits higher power dissipation compared to the others, attributed to the absence of stacking and the presence of excess access transistors. Consequently, the SREWH12T cell draws less current, leading to lower power dissipation.

**Power Results**

v1 from time 0 to 1e-007
Average power consumed -> 2.988363e-007 watts
Max power 2.070744e-003 at time 5.06763e-008
Min power 1.787287e-012 at time 4.6625e-008

**H. New Performance Metric for SRAM Cells**

The relative EQM values presented in Fig. 13 demonstrate that the proposed SREWH12T exhibits the highest EQM among the compared cells, indicating its superior overall performance. This validation reinforces the efficacy of the SREWH12T design in achieving a balance between critical charge, read

stability, write ability, access times, and other important metrics. Consequently, SREWH12T emerges as a promising candidate for various applications, particularly in scenarios where robustness, efficiency, and reliability are paramount considerations.

$$EQM = \frac{Q_C \times \text{RSNM} \times \text{WWTV}}{E_{\text{READ}} \times E_{\text{WRITE}} \times H_{\text{PWR}} \times \text{Area}}.$$

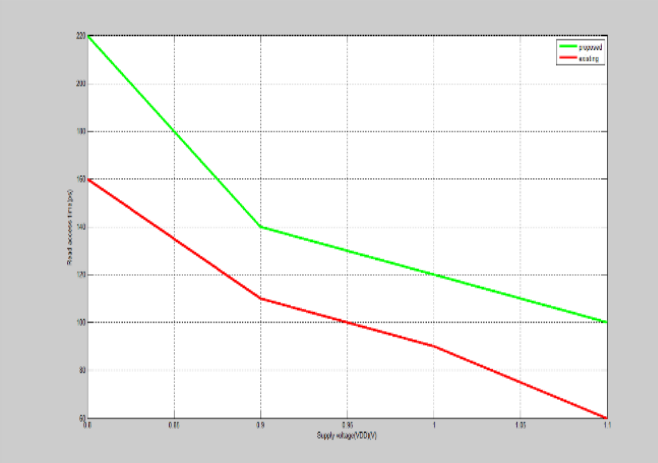


**Figure 4: TRA of comparison cell at different VDDs**

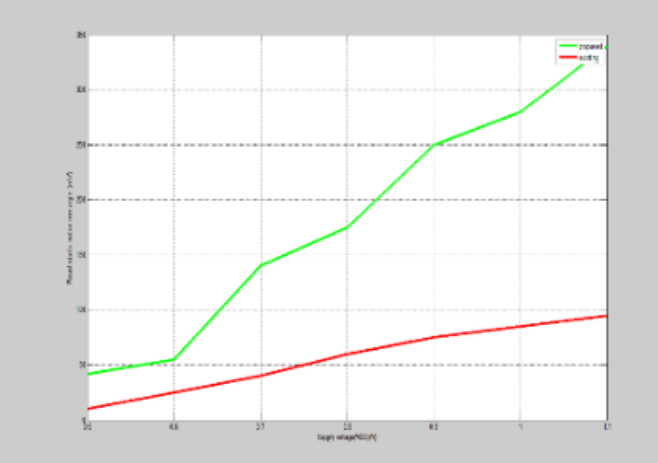


**Figure 5: RSNM of all the comparison cell at different VDDs.**

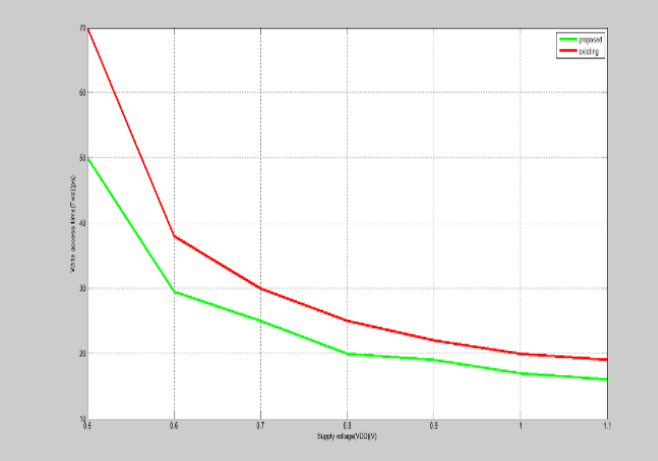


**Figure 6: TWA of all the considered cell at different VDDs**

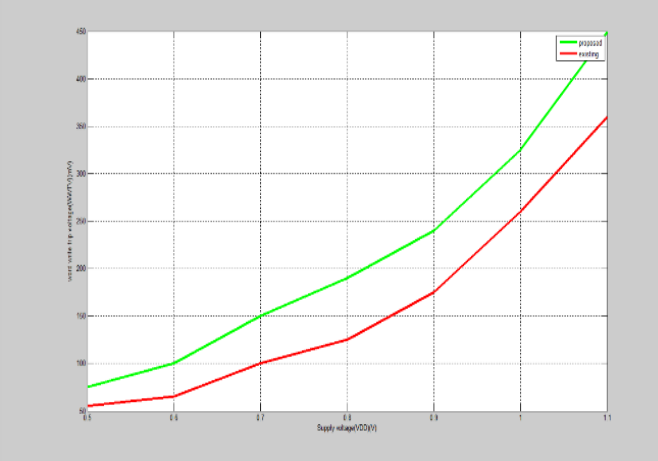


**Figure 7: WWTV of all the comparison cells at different VDDs.**

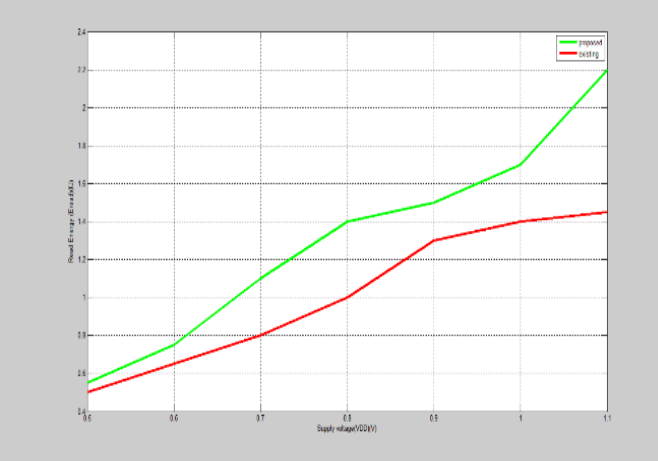


**Figure 8: Energy consumption during read mode (E READ) at different VDDs**

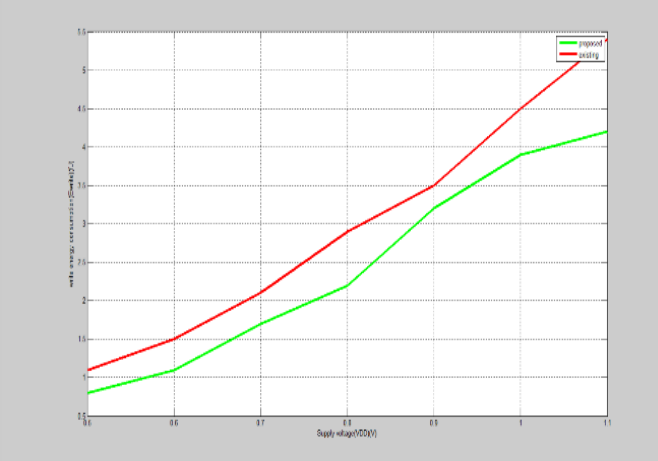


**Figure 9: Energy consumption during write mode (E WRITE) at different VDDs.**

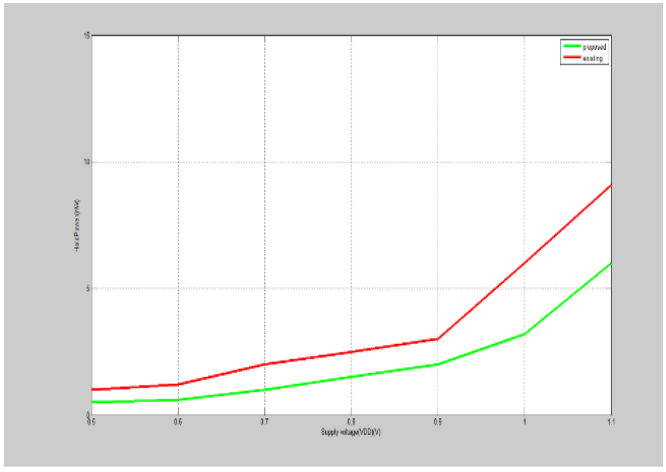


**Figure 10: HPWR of all the considered cells at various VDDs.**

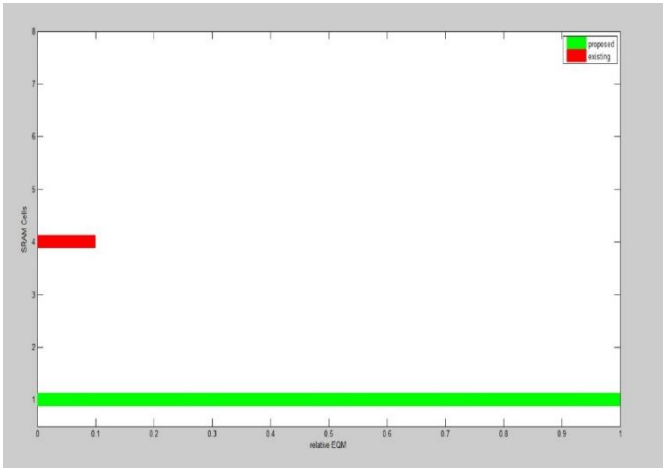


**Figure 11: Relative EQM with respect to SREWH14T at VDD=1V.**

### F. Soft-Error Recovery Simulations and Comparison

To simulate a single-event upset (SEU) and evaluate the proposed cell's resilience to soft errors, a double exponential current source is utilized. The orientation of this current source is configured to induce a negative transient pulse at the drain of an NMOS transistor (as depicted in Fig. 12) and a positive transient pulse at the drain of a PMOS transistor (as illustrated in Fig. 13).

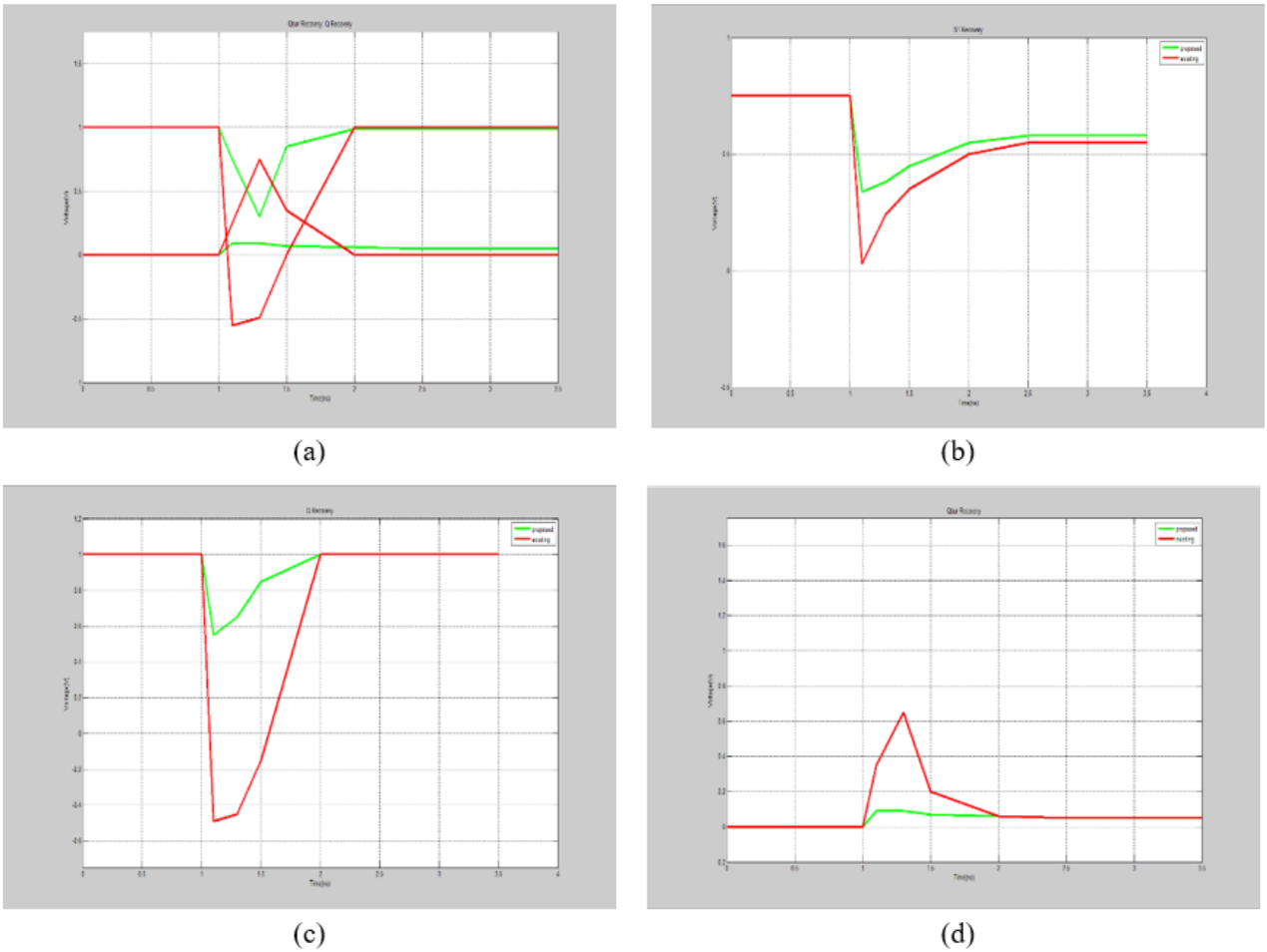
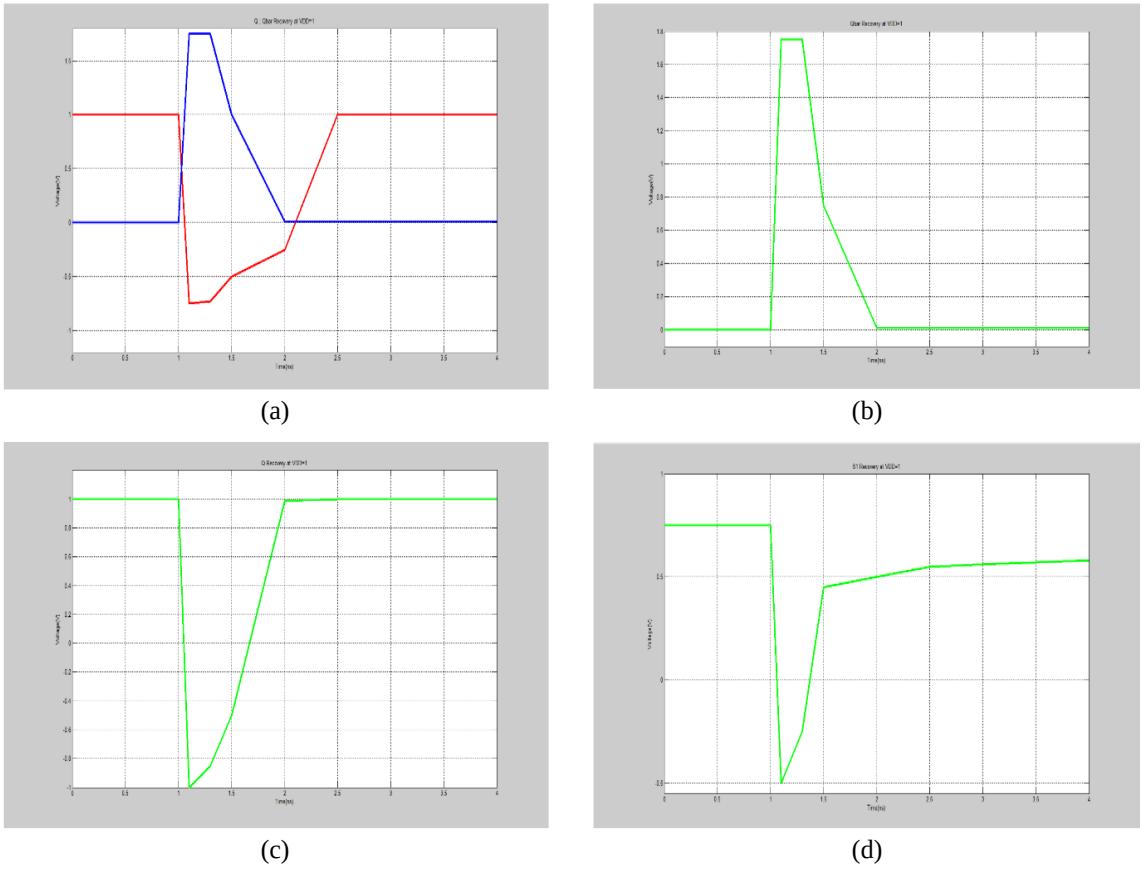



**Fig 12: Behavior of soft-error recovery when different amounts of charge are collected. (a) Behavior of Q-Q bar (b) Behavior of s1 (c) Behavior of Q (d). Behavior of Q bar.**



(a) (b)

(c) (d)

**Fig 13: Recovery of SREWH12T when storage node-pair Q-QB are affected by SEUs at VDD=1V (a) Storage node-pair Q-QB (b) Node Q (C) Node QB (d) Node S1.**

## V. CONCLUSION

We introduce SREWH12T, Soft-Error Reduction and Enhancement of Write Stability and Hold Power Optimization by using 12T SRAM designed specifically for aerospace applications. SREWH12T demonstrates remarkable resilience against radiation-induced soft errors, with the ability to restore its original data at all sensitive nodes even in the event of radiation strikes. Moreover, the cell exhibits robustness against multi-node upsets, further enhancing its reliability in harsh environments. SREWH12T boasts with its exceptional read stability, evident through its superior RSNM, and its minimal hold power consumption in comparison to other cells being evaluated. These collective characteristics make the SREWH12T cell an attractive option for aerospace applications, where maintaining data integrity, minimizing power usage, and withstanding radiation-induced errors are critical considerations. The SREWH12T cell demonstrate reduced EWRITE because of their significantly diminished dynamic power usage. max power required by the SREWH12T SRAM is 2.070744e-003 at time 5.06763e-008.The proposed SREWH12T cell offers a comprehensive solution to the challenges faced in aerospace applications, making it a superior choice over existing contemporary cells. Its exceptional performance across various metrics, coupled with its ability to with stand radiation-induced soft errors, solidifies its suitability for deployment in demanding aerospace environments.

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