

# Review of Multilevel Level Inverter Using Different Topologies

**Omkar S. Lambat<sup>1</sup>, Chandan P. Kolhe<sup>2</sup>, Mohini Y. Sonawane<sup>3</sup>,  
Mangala R. Dhotre<sup>4</sup>**

<sup>4</sup>Assistant Professor, Electronics and Telecommunication Engineering, Government College of Engineering Jalgaon, Maharashtra, India

<sup>1,2,3</sup>Student, Electronics and Telecommunication Engineering, Government College of Engineering Jalgaon, Maharashtra, India

## Abstract

This paper provides a concise overview of various multilevel inverter (MLI) topologies. The conventional two-level Voltage Source Inverter (VSI) necessitates a filter to generate sinusoidal output waveforms, which can be challenging at high frequencies due to switching losses. To address this issue, multilevel inverters offer lower switching frequencies and reduced total harmonic distortion (THD), eliminating the need for filters and large transformers.

Moreover, a few advantages of MLI inverters are reduced switching losses, better performance at high switching frequencies, and higher power quality (almost pure sinusoidal). Nevertheless, adding to the complexity of the system is the requirement for each switch to have its own gate driver in order to perform MLI. Thus, it's imperative to decrease the MLI's number of switches. In order to reduce the number of switches needed, this paper reviews some of the various current topologies.

Applications such as voltage regulation, VAR compensation, harmonic filtering in power systems, and user interface for renewable energy have led to the development of cascaded H-bridge multilevel inverters. For solar applications, a modified cascaded H-bridge multilevel inverter (MLI) is used. Cascaded H-bridge topology multilevel inverter will aid in reducing the number of switches. Comparing this concept to other multilevel inverters, the switching complexity is reduced.

**Keyword:** MLI (Multilevel Inverter), THD (Total Harmonic Distortion), CHB (Cascaded H-Bridge)

## 1. Introduction:

Applications for inverters include battery storage, solar panels, electric vehicles, air conditioning, uninterruptible power supplies (UPS), and high-voltage direct current (HVDC) transmission lines [1, 2]. Square-wave inverters, sinusoidal two-level pulse width modulation (PWM) inverters, and multilevel inverters are the three types of inverters [3, 4]. The study shows that the variety of renewable energy sources and the scarcity of fossil fuels have led to a surge in power electronics, DC-DC converters, and inverters.

The high cost of renewable energy sources means that the converters need to be extremely dependable, efficient, and perform exceptionally well [5]. It needs to produce output waveforms that are sinusoidal and synchronized with the national power grid [6]. Figure 1 shows the circuit diagram of a two-level

inverter. Whenever SW1 is turned on,  $V_0 = +(V_{dc}/2)$  and  $V_0 = -(V_{dc}/2)$  when SW2 is turned on. It goes without saying that, as Figure 2 illustrates, traditional two-level inverters without pulse width modulation (PWM) provide a square wave output voltage of two levels. With considerable switching losses, this conventional inverter operates at a high switching frequency for high-power applications. Other problems include harmonic distortion and overstressing power semiconductors. These problems make it impractical to connect power electronic switches to the high-voltage grid [10, 11]. These problems require the use of MLI inverters with various topologies. MLI inverters have various advantages such as reduced harmonic distortion, higher power quality (almost pure sinusoidal), less switching losses, and better performance at high switching frequencies [3, 12]. The complexity of the system is increased by the requirement for each switch to have its own gate driver in order to implement MLI. Thus, it is imperative to decrease the quantity of MLI switches [3, 13, 14]. In this paper, several of the various current topologies with fewer switches are reviewed.

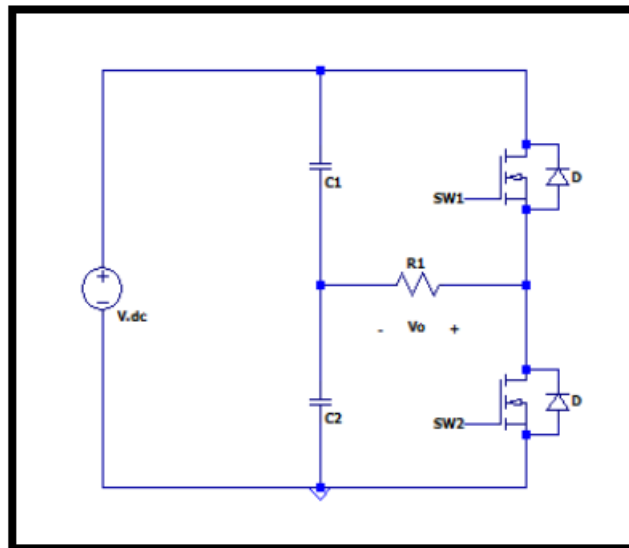


Figure 1.1:- Diagram of a two level inverter

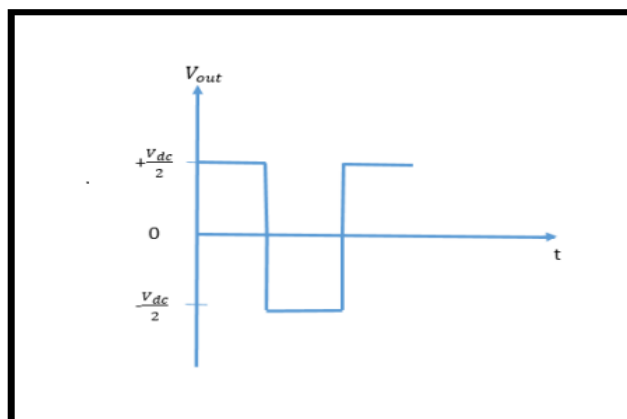


Figure 1.2:- The output voltage of a two-level inverter

The family of converters known as multilevel inverters (MLIs) has enormous potential for use in future research and development. In the field of power engineering, they have a variety of uses. Variable speed drives, renewable energy systems (RES), flexible alternating current transmission systems (FACTS), high voltage direct current (HVDC) transmission, electric vehicles (EVs), and more electric aircraft

(MEA) systems are some of the application areas. Nowadays, the fastest-paced depletion of fossil fuels and their detrimental effects on the environment have led to a sharp rise in the production of power through renewable energy resources. The most important step that comes after the integration of several renewable generating units is proper synchronization. Since solar PV systems generate DC voltage, they need an inverter to link to an AC voltage in order to connect to the grid. The pollution elements known as harmonics have an impact on the inverter's output, which causes the power system to collapse. Therefore, it is imperative to design an inverter with decreased harmonic distortion.

Pure sine wave inverters are typically nonexistent in the world. Modified sine wave inverters are therefore an alternative and practically the best choice. Because of this, multilevel inverters, or MLIs, are recognized as being more affordable, dependable, and highly efficient than other kinds of devices. Multilevel inverters are therefore now widely used due to their capacity for voltage operation and function. By utilizing several separate independent DC voltage sources, the multilevel inverter produces the desired output. By using the switching frequency, the inverter's voltage output waveform becomes nearly sinusoidal as the number of sources increases. Because there are multiple dc sources, it exhibits low voltage stress and low switching losses. A three-level inverter is where the word "multilevel" originates. Because multilevel inverters are well suited to handle the increased need for power rating and power quality associated with fewer switches and lower electromagnetic interference, they are becoming more and more popular in power electronic applications. Multilevel inverters with high switching frequency pulse width modulation (PWM) have a number of benefits over traditional two-level inverters. MLIs have improved sinusoidal output compared to 2-level inverters, which reduce Total Harmonic Distortion (THD) and hence the need for filters. They also have higher efficiency, modularity, and less stress on power electronic components. The flying capacitor (FC) MLI, neutral point clamped (NPC) MLI, and cascaded H-bridge (CHB) MLI are the three classical topologies of MLIs that have been proposed in the literature. Each of these topologies has multiple variants. One issue with the NPC topology is that it needs a considerable amount of clamping diodes that form the output voltage waveform at higher levels.

When more levels are produced, requiring a significant number of capacitors, FC MLI becomes costly and unreliable and causes the issue of capacitor voltage balancing. The CHB MLI is distinct in that it uses several different DC sources, providing modularity and compatibility with fuel cells, solar PV modules, and batteries for power. The CHB MLI requires fewer diodes and capacitors than the other classical topologies.

## 2. Different MLI Topologies:-

A multilevel inverter generates a smooth sinusoidal waveform from multiple dc input sources. Additionally, multi-level inverters are crucial for industrial applications requiring high power. Multilevel inverters with diode-clamped, flying capacitor, and cascaded H bridge topologies are the most popular designs. The multilevel inverter scheme is shown.

Different MLI Topologies are

- Diode-Clamped Topology
- Flying Capacitor Topology
- Cascade H bridge Topology

### 3. Diode-Clamped Topology:-

A diode-clamped Multi-level inverter (n level) uses diodes to produce n voltage levels at the output. Typically, the dc-link bus has (n-1) capacitors. A three-level half-bridge diode clamped multilevel inverter is depicted in the figure. An n-level inverter requires (n1) balancing capacitors, 2(n-1) switches and (n-1) (n-2) clamping diodes. As a result, as Figure illustrates, the three-level classical diode clamped inverter has two capacitors at the DC bus, four switches, and two clamping diodes in addition to producing three levels of voltage at the output.[18,19,20,21,22]

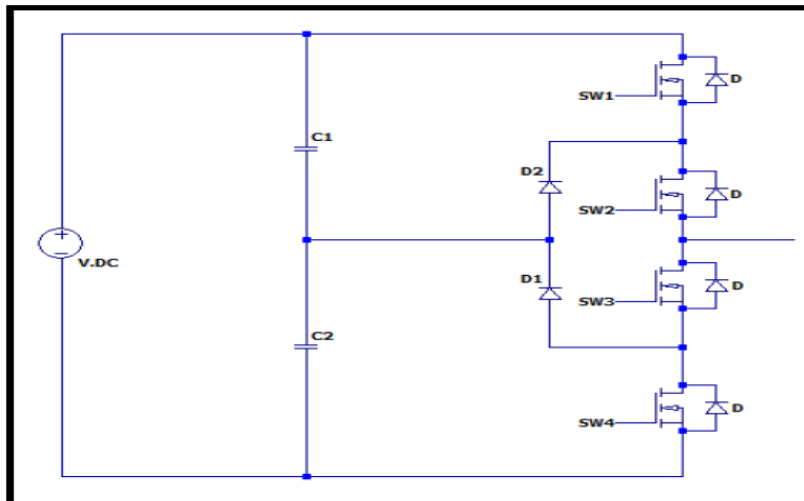


Figure 3.1:- Three level Diode-Clamped MLI

According to the figure three-level inverters provide a square wave output voltage of three levels,

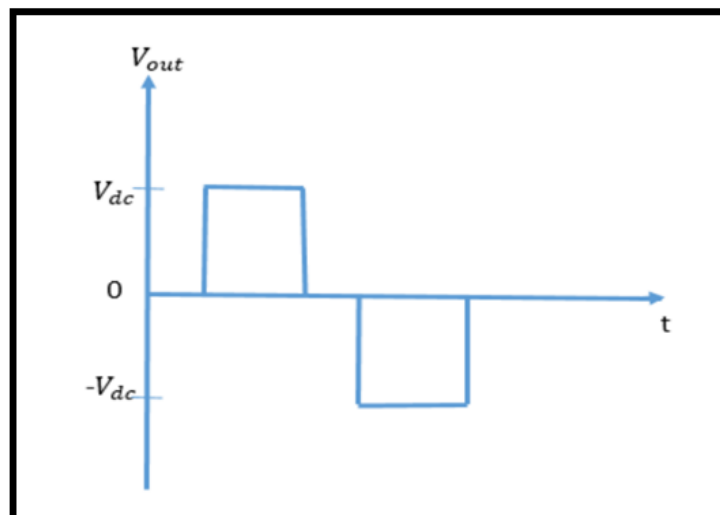


Figure 3.2:- Output waveform of three level diode clamped MLI

The benefits and drawbacks of diode clamped MLI are as follow[23-25]:

#### Benefits:

- The real and reactive power flow can be controlled
- Filters are not required to decrease harmonics.

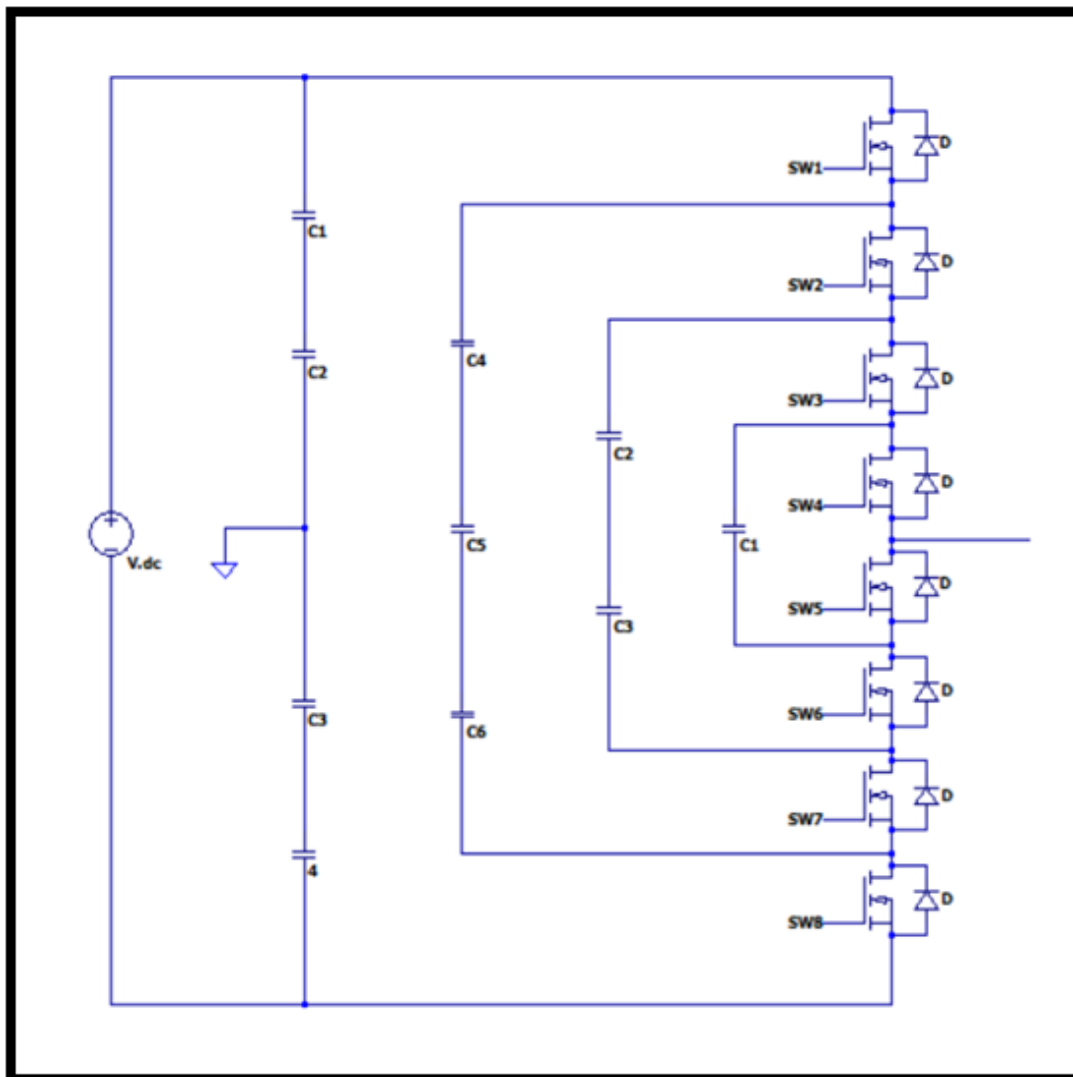
- The voltage of the switch is just half of the voltage of the dc-link
- The voltage of the switch is just half of the voltage of the dc-link

**Drawbacks:**

- Clamping diodes are increased when each level is raised.
- Clamping diodes are increased when each level is raised.

**4. Flying Capacitor Topology:-**

This topology differs from the diode-clamped MLI topology in that the voltage is restricted in this instance by the use of capacitors. The clamped inverter with a capacitor has the same voltage level as the clamped inverter with a diode. One needs  $(n-1)$  capacitors for the dc bus,  $(n-1)(n-2)$  number of flying capacitors, and the total number of  $(n-1)$  switches for an  $n$ -level inverter. A five-level flying capacitor MLI, for example, has four capacitors at the DC bus, eight switches, six clamping capacitors, and five voltage levels at the output[26-31], as shown in Figure.



**Figure 4.1:- Five-level flying capacitor MLI**

According to the figure five-level inverters provide a square wave output voltage of five level,

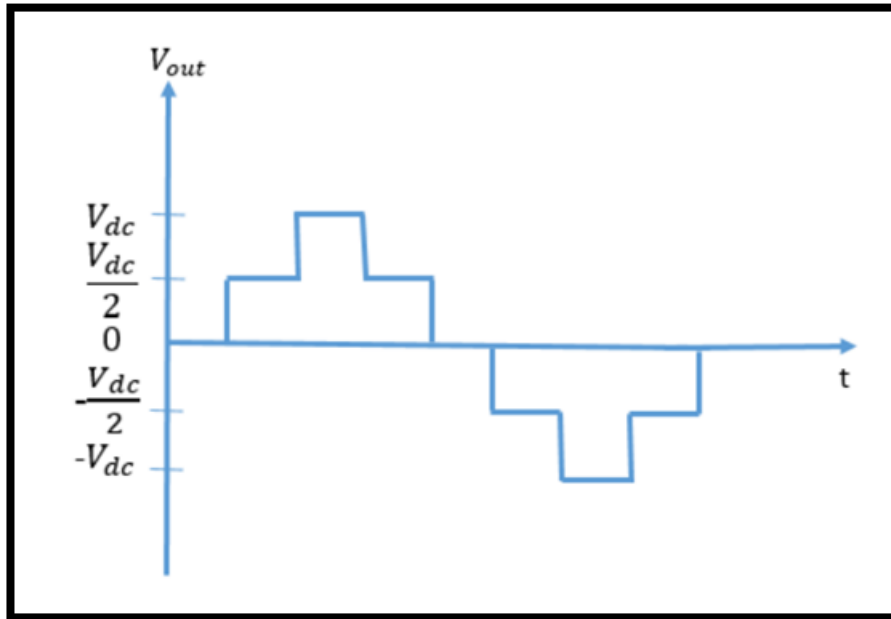


Figure 4.2:-The output waveform of five-level flying capacitor MLI

The benefits and drawbacks of diode clamped MLI are as follow [32-34]:

**Benefits:**

- Filters are not required to decrease harmonics.
- Get rid of the clamping diode problems.
- Reduces the amount of stress on the semiconductor switches.
- It provides the correct switching combination for balancing various voltage levels.
- It is possible to control both real and reactive power flow.

**Drawbacks:**

- Controlling the voltage across all of the capacitors is hard to achieve.
- A decrease in switching efficiency.

**5. Cascaded H-Bridge Topology:-**

A cascaded MLI is made up of a series of H-bridge inverters that have separate DC sources[35-37]. The output voltage of this inverter has a voltage level of  $2s+1$ , where S is the number of DC inputs. As a result, the output voltage levels equal the total voltages produced by each H-bridge cell. Each cell has three voltage levels, and the cascaded MLI is composed of linked H-bridge cells in series[35-41].

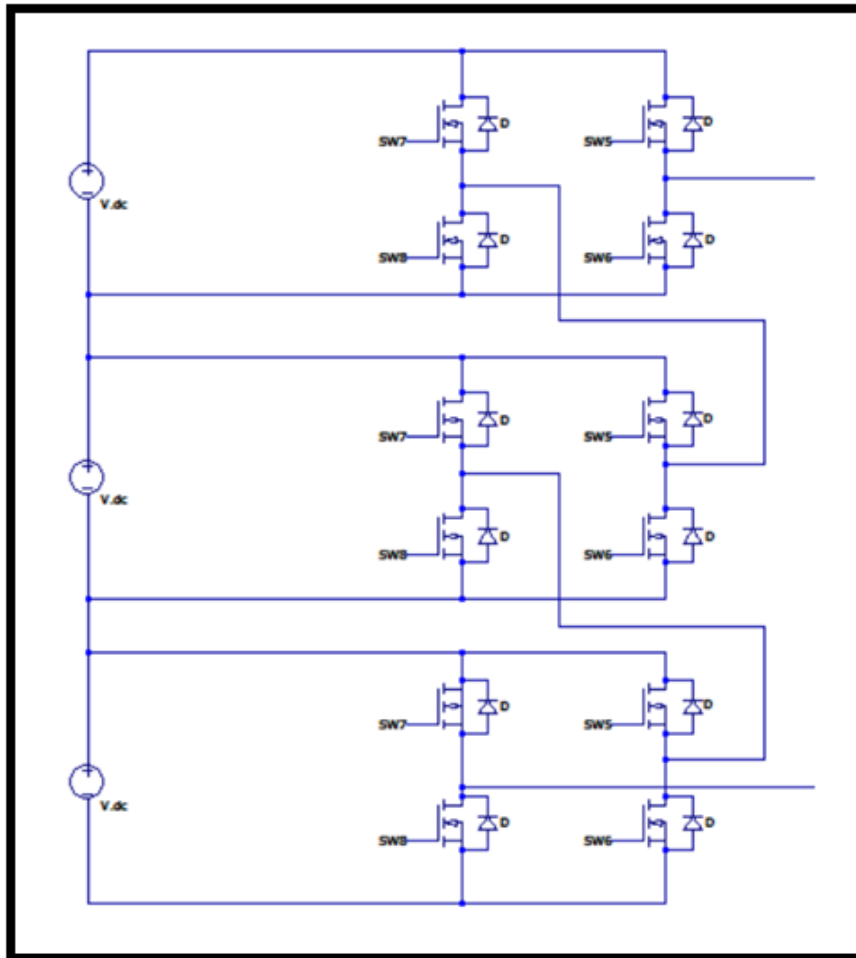


Figure 5.1:- Seven-level H-bridge MLI [42]

According to Figure the seven-level cascaded inverters provide a square wave output voltage of seven levels without employing PWM.

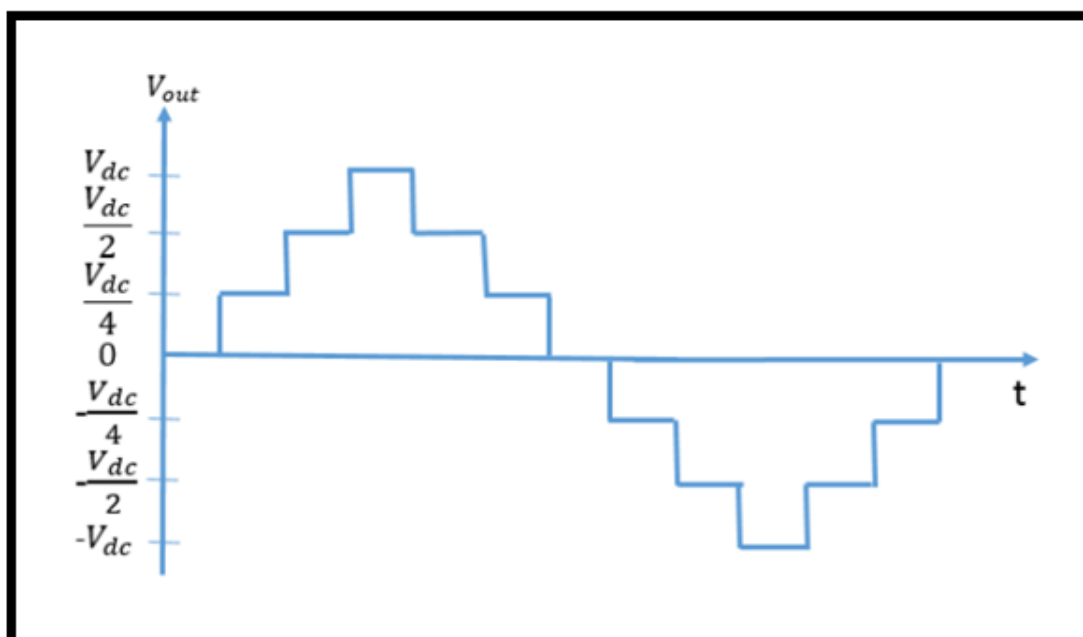


Figure 5.2:-The output waveform of seven-level cascaded MLI

The benefits and drawbacks of cascaded H bridge MLI are as follow[42-44]:

**Benefits:**

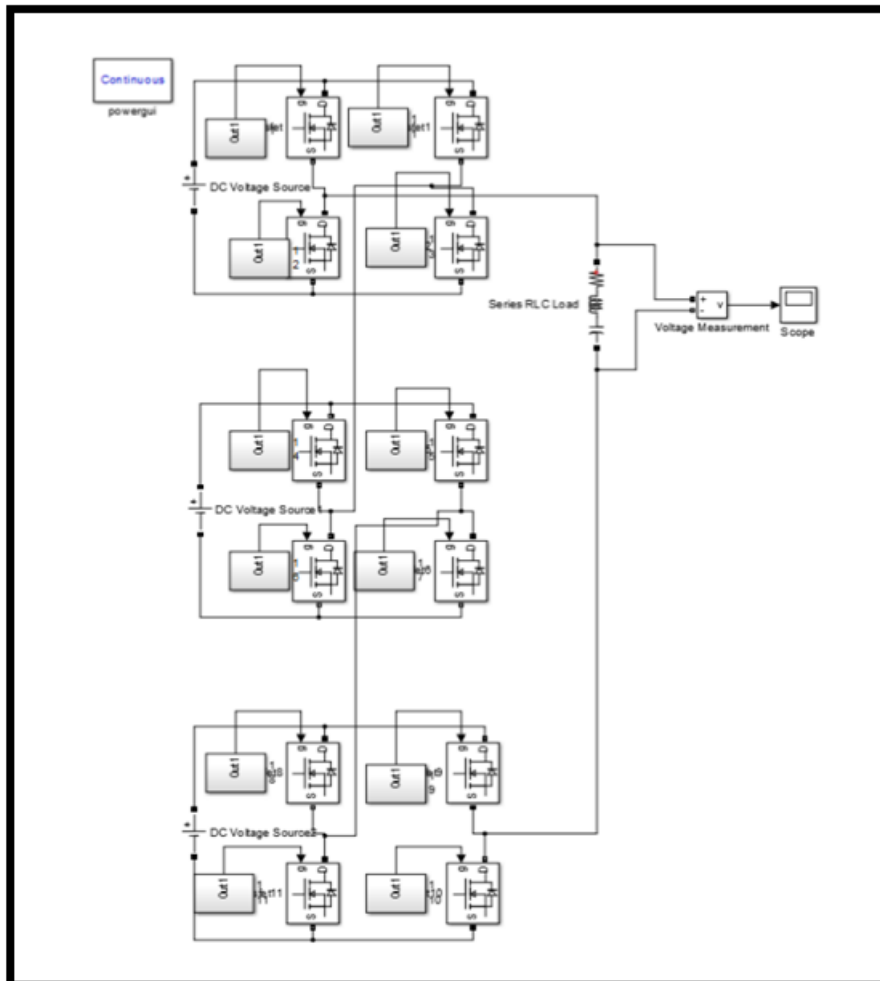
- To decrease switching losses, a soft switching approach can be employed
- Filters are not required to decrease harmonics.
- THD (total harmonic distortion) is extremely low
- A lower number of components is used in this MLI

**Drawbacks:**

- For power conversions, it requires independent dc sources.

**6. Cascaded H-Bridge Topology For 15 Level Multilevel Inverter:-**

An inverter that uses multiple H-bridge circuits connected in series, or "cascaded," to produce a higher number of voltage levels is known as a 15 cascaded H-bridge asymmetrical multilevel inverter. The term "asymmetrical" describes how the voltage levels generated by the inverter are not symmetrical around a midpoint, unlike what would happen in a conventional inverter [49].



**Figure 6.1:- Circuit Diagram For 15 Level Cascade H Bridge MLI[49]**

An H-bridge is a circuit configuration that allows for the direction of current flow through a load to be reversed by switching the polarity of the voltage applied to the load. By cascading multiple H bridges together and controlling the individual switches in each one, a multilevel inverter can produce a much larger number of voltage levels than a traditional inverter. A large number of voltage levels can be



produced by connecting 15 H-bridge circuits in series to create a 15 cascaded H-bridge asymmetrical multilevel inverter. The inverter's asymmetrical feature, which can be advantageous in some situations, describes how the voltage levels it produces are not symmetrical around a midpoint.

	0	5	10	15	20	25	30	35	30	25	20	15	10	5	0	-5	-10	-15	-20	-25	-30	-35	-30	-25	-20	-15	-10	-5	
	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	
s1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0
s2	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
s3	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0
s4	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
s5	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0
s6	1	1	0	0	1	1	0	0	1	1	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
s7	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	1	1	1	0	0	1	1	0	0
s8	0	0	1	1	0	0	1	1	1	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
s9	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	1	1
s10	1	1	1	1	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
s11	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0
s12	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 6.2:- Switching table for 15 level Cascade H Bridge-MLI [49]

The above table is prepared by using certain formulae to get the values.

- Number of steps  $2(N-1)$
- Phase delay =  $\text{period} / \text{total number of steps} * \text{step}$
- Pulse width =  $(\text{number of pulse width} / \text{total number of steps}) * 10$

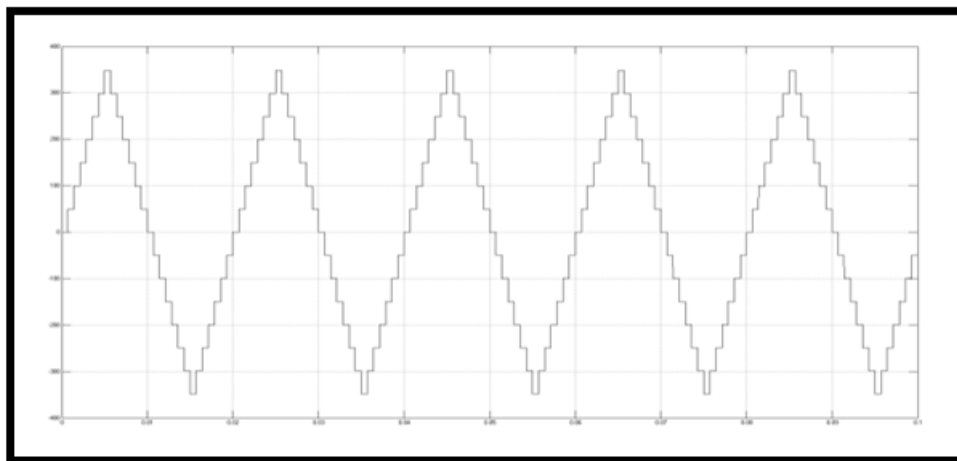


Figure 6.3:- Output Waveform Of 15 Level CHB MLI.[49]

### 7. Cascaded H Bridge Topology For 21 Level Multi-Level Inverter:-

Asymmetrical MLI with 21 levels is composed of 4 H-bridge cells or modules. Every cell or module has four MOSFETS. It has four distinct dc sources of magnitude 10, 20, 30, and 40 volts because it is asymmetrical. Every module or cell is interconnected in a passive series. As seen in figure, various loads, such as R, RL, and RLC loads, are connected across the circuit. The pulse generator provides the gate signal for a MOSFET; the switching mechanism is displayed in the switching table.[48]

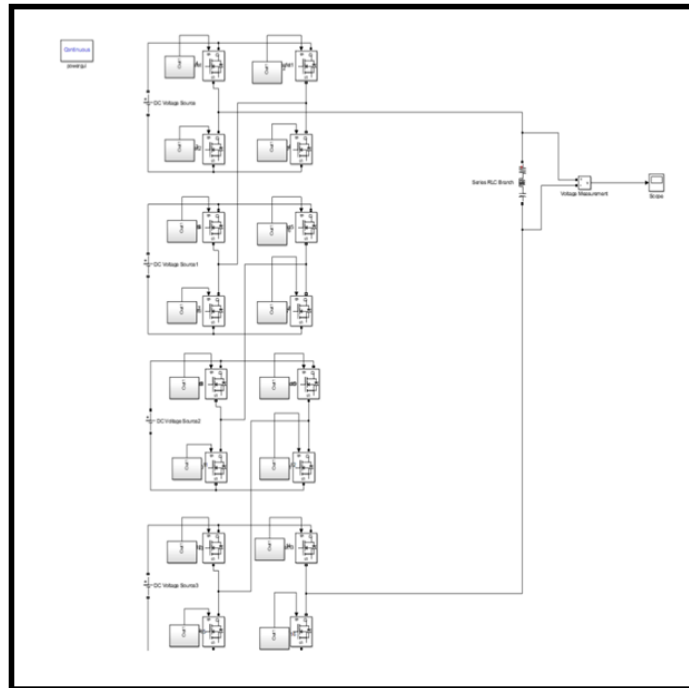


Figure 7.1:- Circuit Diagram For 21 Level Cascade H Bridge MLI.[48]

1	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39		
2	0	10	20	30	40	50	60	70	80	90	100	90	80	70	60	50	40	30	20	10	0	-10	-20	-30	-40	-50	-60	-70	-80	-90	-100	-90	-80	-70	-60	-50	-40	-30	-20	-10		
3	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0
4	2	1	0	1	1	0	1	1	0	1	1	0	1	1	0	1	1	0	1	1	0	1	1	0	1	1	0	1	1	0	1	1	0	1	1	0	1	1	0	1	1	0
5	3	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1	0	0	1	0	0	1	0	0	1	0	0	1	0	0	1	0	0	
6	4	0	1	0	0	1	0	0	1	0	0	1	0	0	1	0	0	1	0	0	1	0	0	1	0	0	1	0	0	1	0	0	1	0	0	1	0	0	1	0	0	
7	5	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	
8	6	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	
9	7	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1	0	0	1	0	0	1	0	0	1	0	0	1	0	0	1	0	0	
10	8	0	1	0	0	1	0	0	1	0	0	1	0	0	1	0	0	1	0	0	1	0	0	1	0	0	1	0	0	1	0	0	1	0	0	1	0	0	1	0	0	
11	9	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	
12	10	1	1	0	1	1	1	0	0	0	0	1	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	
13	11	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1	0	0	1	0	0	1	0	0	1	0	0	1	0	0	1	0	0	
14	12	0	0	1	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	
15	13	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
16	14	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	
17	15	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	
18	16	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	

Figure 7.2:- Switching table for 21 level Cascade H Bridge-MLI

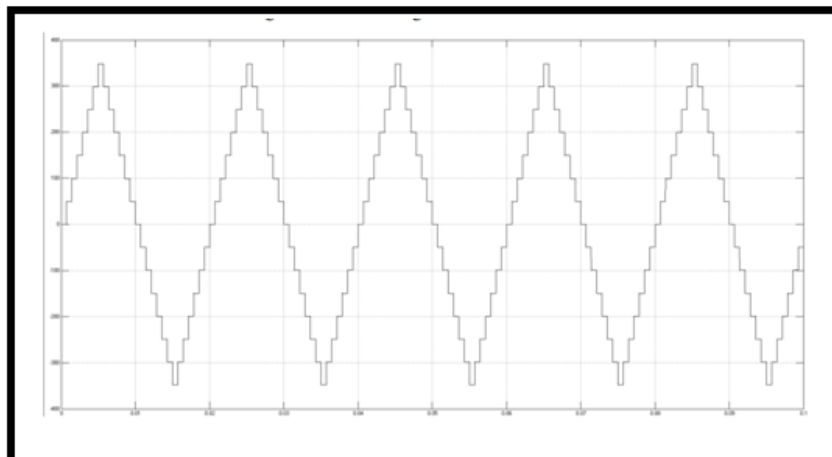
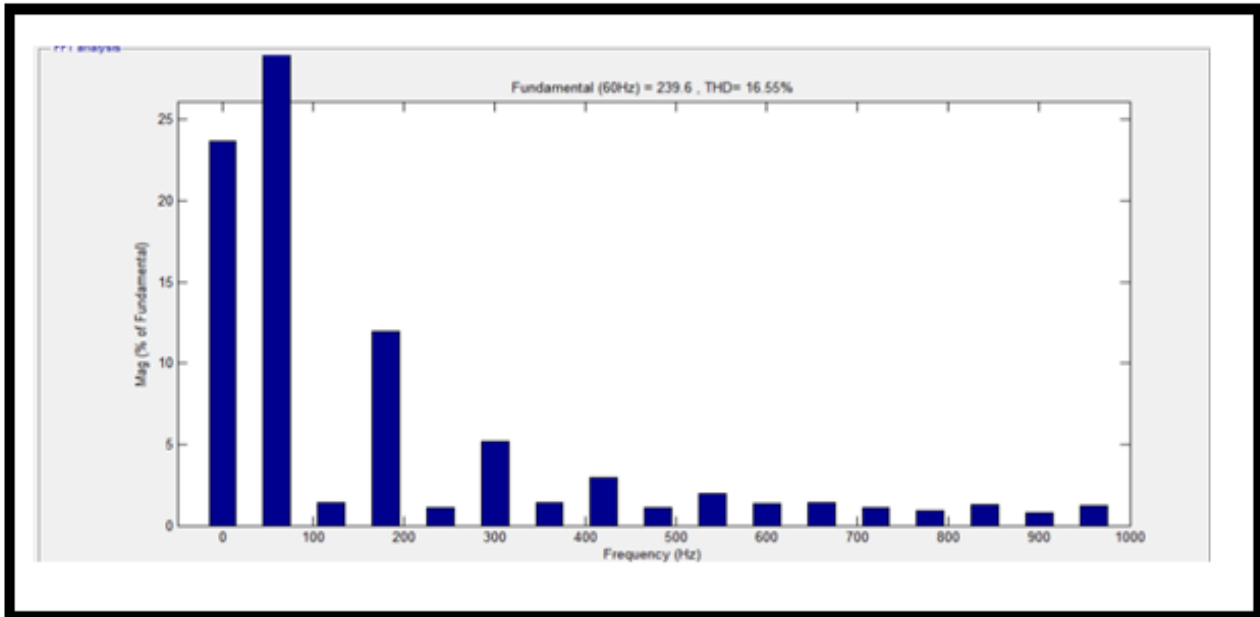
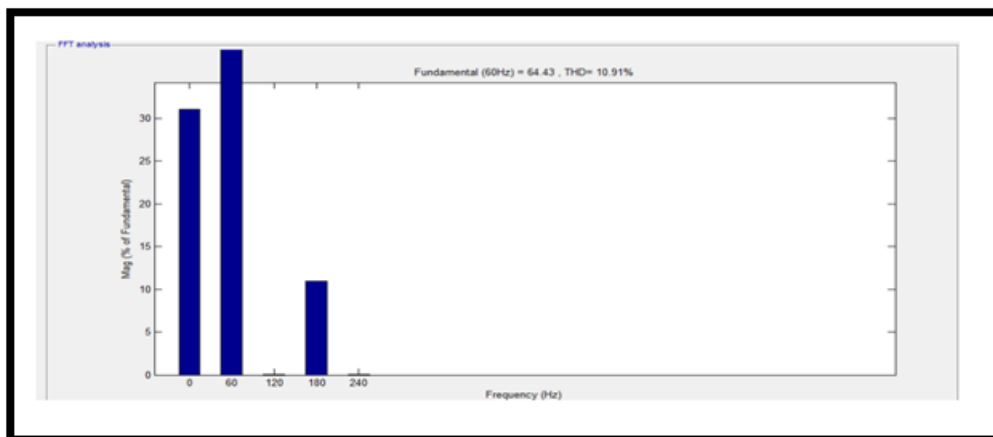


Figure 7.3 :- Output Waveform Of 21 Level CHB MLI.[48]

**8. THD ANALYSIS OF 15-LEVEL, 21-LEVEL CHB MLIs:-**



**Figure 8.1:- THD for level 15 [50]**



**Figure 8.2:- THD for level 21[50]**

Multilevel inverter	No. of Semiconductor switches	THD%
15-level CHB MLI	12	16.55%
21-level CHB MLI	16	10.91%

**Table 8.3:-Analysis of Cascaded H Bridge MLI for proposed levels**

**9. Conclusion:**

This paper present comparative study of various topologies of the multilevel inverter. Diode Clamped Multilevel inverter DC level will discharge when control and monitoring are not precise and Number of clamping diodes increases with increases of each level and In Flying capacitor multilevel inverter voltage control is difficult for all the capacitors and has poor switching efficiency. [42-45]. The CHB MLI for 15 and 21 level multilevel inverter with minimized number of semiconductor switches by using pulse generators has been implemented by M. Navya Sri, Mohd Abdul Wasi , N. Sathish , K. Bhargav

Prasad CHB MLI are used extensively because of their better quality output voltage waveforms as compared to other types of MLIs. This paper gives THD of 16.55% for 15-level CHB MLI, 10.91% for 21-level and 8.26%. The proposed inverters are used integration of Renewable Energy Sources, FACTS, HEVs, Power quality improvements. [48-50].

## 10. References:

1. Kjaer, S. B., Pedersen, J. K., & Blaabjerg, F. (2005). A review of single-phase grid-connected inverters for photovoltaic modules. *IEEE Transactions on Industry Applications*, 41(5), 1292–1306. doi:10.1109/TIA.2005.853371.
2. Vázquez, N., & López, J. V. Inverters. (2008). In *Power Electronics Handbook* (pp. 289–338). Elsevier.
3. Malinowski, M., Gopakumar, K., Rodriguez, J., & Perez, M. A. (2009). A survey on cascaded multilevel inverters. *IEEE Transactions on Industrial Electronics*, 57(7), 2197–2206. doi:10.1109/TIE.2009.2030767.
4. Rodriguez, J., Lai, J.-S., & Peng, F. Z. (2002). Multilevel inverters: a survey of topologies, controls, and applications. *IEEE Transactions on Industrial Electronics*, 49(4), 724–738.
5. Mirafzal, B., & Adib, A. (2020). On Grid-Interactive Smart Inverters: Features and Advancements. *IEEE Access*, 8, 160526–160536. doi:10.1109/ACCESS.2020.3020965
6. Lasseter, R. H., Chen, Z., & Pattabiraman, D. (2020). Grid-Forming Inverters: A Critical Asset for the Power Grid. *IEEE Journal of Emerging and Selected Topics in Power Electronics*, 8(2), 925–935. doi:10.1109/JESTPE.2019.2959271.
7. Aghazadeh, A., Davari, M., Nafisi, H., & Blaabjerg, F. (2019). Grid integration of a dual two-level voltage-source inverter considering grid impedance and phase-locked loop. *IEEE Journal of Emerging and Selected Topics in Power Electronics*.
8. Aghazadeh, A., Khodabakhshi-Javinani, N., Nafisi, H., Davari, M., & Pouresmaeil, E. (2019). Adapted near-state PWM for dual two-level inverters in order to reduce common-mode voltage and switching losses. *IET Power Electronics*, 12(4), 676–685. doi:10.1049/iet-pel.2018.5268.
9. Aghazadeh, A., Jafari, M., Khodabakhshi-Javinani, N., Nafisi, H., & Namvar, H. J. (2018). Introduction and advantage of space opposite vectors modulation utilized in dual two-level inverters with isolated DC sources. *IEEE Transactions on Industrial Electronics*, 66(10), 7581-7592. <https://doi.org/10.1109/TIE.2018.2880720>
10. Gupta, K. K., & Bhatnagar, P. (2017). Multilevel inverters: Conventional and emerging topologies and their control. In *Multilevel Inverters: Conventional and Emerging Topologies and Their Control*. Academic Press. doi:10.1016/C2016-0-03360-0.
11. Ponraj, R. P., & Sigamani, T. (2021). A novel design and performance improvement of symmetric multilevel inverter with reduced switches using genetic algorithm. *Soft Computing*, 25(6), 4597–4607. doi:10.1007/s00500-020-05466-7.
12. Ali, A. N., Jeyabharath, R., & Udayakumar, M. D. (2016). Cascaded Multilevel Inverters for Reduce Harmonic Distortions in Solar PV Applications. *Asian Journal of Research in Social Sciences and Humanities*, 6(11), 703. doi:10.5958/2249-7315.2016.01223.5.
13. Kouro, S., Rebolledo, J., & Rodríguez, J. (2007). Reduced switching-frequency-modulation algorithm for high-power multilevel inverters. *IEEE Transactions on Industrial Electronics*, 54(5), 2894–2901. doi:10.1109/TIE.2007.905968.

14. Gautam, S. P., Sahu, L. K., & Gupta, S. (2016). Reduction in number of devices for symmetrical and asymmetrical multilevel inverters. *IET Power Electronics*, 9(4), 698–709. doi:10.1049/iet-pel.2015.0176.
15. Nguyen, N. V., Nguyen, T. K. T., & Lee, H. H. (2014). A reduced switching loss PWM strategy to eliminate common-mode voltage in multilevel inverters. *IEEE Transactions on Power Electronics*, 30(10), 5425–5438. <https://doi.org/10.1109/TPEL.2014.2377152>.
16. Chowdhury, M. R., Rahman, M. A., Islam, M. R., & Mahfuz-Ur-Rahman, A. M. (2021). A New Modulation Technique to Improve the Power Loss Division Performance of the Multilevel Inverters. *IEEE Transactions on Industrial Electronics*, 68(8), 6828–6839. doi:10.1109/TIE.2020.3001846.
17. Keddar, M., Doumbia, M. L., Krachai, M. Della, Belmokhtar, K., & Midoun, A. H. (2019). Interconnection performance analysis of single phase neural network based NPC and CHB multilevel inverters for grid-connected PV systems. *International Journal of Renewable Energy Research*, 9(3), 1451–1461.
18. Hossam-Eldin, A. A., Negm, E., Elgamal, M. S., & AboRas, K. M. (2020). Operation of grid-connected DFIG using SPWM and THIPWM-based diode-clamped multilevel inverters. *IET Generation, Transmission and Distribution*, 14(8), 1412–1419. doi:10.1049/iet-gtd.2019.0248.
19. Wu, B. and M. Narimani, (2016). Diode-Clamped Multilevel Inverters in High-Power Converters and AC Drives, 143–183. doi:10.1002/9781119156079.ch8.
20. Choudhury, S., Nayak, S., Dash, T. P., & Rout, P. K. (2018). A comparative analysis of five level diode clamped and cascaded H-bridge multilevel inverter for harmonics reduction. In *International Conference on Technologies for Smart City Energy Security and Power: Smart Solutions for Smart Cities, ICSESP 2018 - Proceedings (Vols. 2018-January)*, 1–6. IEEE. doi:10.1109/ICSESP.2018.8376690.
21. Narendra Rao, P., & Nakka, J. (2019). A Novel Hybrid Multilevel PWM Technique for Power Rating Enhancement in Improved Hybrid Cascaded Diode Clamped Multilevel Inverter. *Electric Power Components and Systems*, 47(11–12), 1132–1143. doi:10.1080/15325008.2019.1659455.
22. Shi, S., Wang, X., Zheng, S., Zhang, Y., & Lu, D. (2018). A new diode-clamped multilevel inverter with balance voltages of DC capacitors. *IEEE Transactions on Energy Conversion*, 33(4), 2220–2228. doi:10.1109/TEC.2018.2863561.
23. Hassan, P. D. R., & Shyaa, S. S. (2021). Simulink Implementation of Voltage Stability Improvements Using STATCOM based 5-level Diode Clamped Converter. *IOP Conference Series: Materials Science and Engineering*, 1105(1), 012009. doi:10.1088/1757-899x/1105/1/012009.
24. Adam, G. P., Finney, S. J., Massoud, A. M., & Williams, B. W. (2008). Capacitor balance issues of the diode-clamped multilevel inverter operated in a quasi-two-state mode. *IEEE Transactions on Industrial Electronics*, 55(8), 3088–3099. doi:10.1109/TIE.2008.922607.
25. Von Bloh, J., & De Doncker, R. W. (2002). Design rules for diode-clamped multilevel inverters used in medium-voltage applications. *International Power Electronics Congress - CIEP, 2002-January*, 165–170. doi:10.1109/CIEP.2002.1216654.
26. Escalante, M. F., Vannier, J. C., & Arzandé, A. (2002). Flying capacitor multilevel inverters and DTC motor drive applications. *IEEE Transactions on Industrial Electronics*, 49(4), 809–815. doi:10.1109/TIE.2002.801231.
27. Humayun, M., Khan, M. M., Hassan, M. U., & Zhang, W. (2021). Analysis of hybrid switches symmetric flying capacitor multilevel inverter based STATCOM. *International Journal of Electrical*

- Power and Energy Systems, 131, 107054. doi:10.1016/j.ijepes.2021.107054.
28. Coday, S., Barchowsky, A., & Pilawa-Podgurski, R. C. N. (2021). A 10-level gan-based flying capacitor multilevel boost converter for radiation-hardened operation in space applications. Conference Proceedings - IEEE Applied Power Electronics Conference and Exposition - APEC, 2798–2803. doi:10.1109/APEC42165.2021.9487143.
  29. Humayun, M., Khan, M. M., Muhammad, A., Xu, J., & Zhang, W. (2020). Evaluation of symmetric flying capacitor multilevel inverter for grid-connected application. International Journal of Electrical Power and Energy Systems, 115, 105430. doi:10.1016/j.ijepes.2019.105430.
  30. Barth, C. B., Assem, P., Foulkes, T., Chung, W. H., Modeer, T., Lei, Y., & Pilawa-Podgurski, R. C. (2019). Design and control of a GaN-based, 13-level, flying capacitor multilevel inverter. IEEE Journal of Emerging and Selected Topics in Power Electronics, 8(3), 2179-2191. <https://doi.org/10.1109/JESTPE.2019.2956166>.
  31. Abhilash, T., Annamalai, K., & Tirumala, S. V. (2019). A Seven-Level VSI with a Front-End Cascaded Three-Level Inverter and Flying-Capacitor-Fed H-Bridge. IEEE Transactions on Industry Applications, 55(6), 6073–6088. doi:10.1109/TIA.2019.2933378.
  32. Amini, J., & Moallem, M. (2017). A Fault-Diagnosis and Fault-Tolerant Control Scheme for Flying Capacitor Multilevel Inverters. IEEE Transactions on Industrial Electronics, 64(3), 1818–1826. doi:10.1109/TIE.2016.2624722.
  33. Porselvi, T., & Muthu, R. (2011). Comparison of cascaded H-bridge, neutral point clamped and flying capacitor multilevel inverters using multicarrier PWM. Proceedings - 2011 Annual IEEE India Conference: Engineering Sustainable Solutions, INDICON-2011. doi:10.1109/INDCON.2011.6139534.
  34. Adam, G. P., Anaya-Lara, O., Burt, G., Finney, S. J., & Williams, B. W. (2009). Comparison between flying capacitor and modular multilevel inverters. IECON Proceedings (Industrial Electronics Conference), 271–276. doi:10.1109/IECON.2009.5414934.
  35. Wu, B., & Narimani, M. (2017). Cascaded H-bridge multilevel inverters.
  36. Chithra, M., & Dasan, S. G. B. (2011). Analysis of cascaded H bridge multilevel inverters with photovoltaic arrays. 2011 International Conference on Emerging Trends in Electrical and Computer Technology, ICETECT 2011, 442–447. doi:10.1109/ICETECT.2011.5760157.
  37. Odeh, C. I., Lewicki, A., & Morawiec, M. (2021). A Single-Carrier-Based Pulse-Width Modulation Template for Cascaded HBridge Multilevel Inverters. IEEE Access, 9, 42182–42191. doi:10.1109/ACCESS.2021.3065743.
  38. Memon, M. A., Siddique, M. D., Saad, M., & Mubin, M. (2021). Asynchronous Particle Swarm Optimization-Genetic Algorithm (APSO-GA) based Selective Harmonic Elimination in a Cascaded H-Bridge Multilevel Inverter. IEEE Transactions on Industrial Electronics. doi:10.1109/TIE.2021.3060645.
  39. Lee, E. J., Kim, S. M., & Lee, K. B. (2020). Modified phase-shifted PWM scheme for reliability improvement in cascaded Hbridge multilevel inverters. IEEE Access, 8, 78130–78139. doi:10.1109/ACCESS.2020.2989694.
  40. Maurya, S., Mishra, D., Singh, K., Mishra, A. K., & Pandey, Y. (2019). An Efficient Technique to reduce Total Harmonics Distortion in Cascaded H- Bridge Multilevel Inverter. Proceedings of 2019 3rd IEEE International Conference on Electrical, Computer and Communication Technologies, ICECCT 2019. doi:10.1109/ICECCT.2019.8869424.

41. Bhatnagar, P., Agrawal, R., & Gupta, K. K. (2019). Reduced device count version of single-stage switched-capacitor module for cascaded multilevel inverters. *IET Power Electronics*, 12(5), 1079–1086. doi:10.1049/iet-pel.2018.6017.
42. Khoucha, F., Ales, A., Khoudiri, A., Marouani, K., Benbouzid, M. E. H., & Kheloui, A. (2010). A 7-level single DC source cascaded H-bridge multilevel inverters control using hybrid modulation. 19th International Conference on Electrical Machines, ICEM 2010. doi:10.1109/ICELMACH.2010.5608179.
43. Lee, E. J., & Lee, K. B. (2021). Performance improvement of cascaded H-bridge multilevel inverters with modified modulation scheme. *Journal of Power Electronics*, 21(3), 541–552. doi:10.1007/s43236-020-00200-w.
44. Tackie, S. N., & Babaei, E. (2020). Modified topology for three-phase multilevel inverters based on a developed H-bridge inverter. *Electronics*, 9(11), 1848. <https://doi.org/10.3390/electronics9111848>.
45. Chamarthi, P. K., Al-Durra, A., El-Fouly, T. H. M., & Jaafari, K. Al. (2021). A Novel Three-Phase Transformerless Cascaded Multilevel Inverter Topology for Grid-Connected Solar PV Applications. *IEEE Transactions on Industry Applications*, 57(3), 2285–2297. doi:10.1109/TIA.2021.3057312.
46. Pallavi Appaso Arbune1 , Dr. Asha Gaikwad Comparative Study of Three level and Five level Inverter.
47. CH. Sajan1 , M. Navya Sri2 , Mohd Abdul Wasi3 , N. Sathish4 , K. Bhargav Prasad5 Implementation of 7-Level and 31-Level Cascaded H-Bridge Multilevel Inverters with Reduced Number of Semiconductor Switches
48. Gayatri Kulkarni1, Prof. P. K. Sankala2 Comparison of Conventional Single Phase 21-level Cascaded H-Bridge Multilevel Inverter and Single Phase 21 Level Multilevel Inverter with Reduced Switches and Sources for Renewable Energy Applications.
49. R.Anand [1] , M.Kamatchi [2] A Fifteen Level Cascaded H-Bridge Multilevel Inverter with Space Vector PWM Technique with Reduced Number of Switches
50. CH. Sajan1 , M. Navya Sri2 , Mohd Abdul Wasi3 , N. Sathish4 , K. Bhargav Prasad5 Implementation of 7-Level and 31-Level Cascaded H-Bridge Multilevel Inverters with Reduced Number of Semiconductor Switches