Review of Low-Power CMOS Full Adder Using Hybrid Logic circuit

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Abstract

Low-power digital circuits play a crucial role in modern VLSI systems, particularly in portable and battery-powered devices. The full adder is a key arithmetic component widely used in arithmetic logic units (ALUs), multipliers, and digital signal processing systems. However, conventional CMOS full adder designs typically involve high power consumption and a large number of transistors.

This paper proposes a low-power CMOS full adder based on hybrid logic techniques. The design integrates multiple logic styles, including complementary CMOS, pass transistor logic, and transmission gate logic, to minimize power usage, reduce propagation delay, and enhance overall performance. Simulation results indicate that the proposed design achieves improved power efficiency and faster operation compared to conventional full adders, making it well-suited for high-performance VLSI applications

1. Introduction

Very Large-Scale Integration (VLSI) technology has made it possible to design highly complex digital systems with enhanced performance and lower power consumption. In today’s electronic devices such as smartphones, laptops, and embedded systems, minimizing power usage has become a critical design objective. Arithmetic circuits, especially full adders, are fundamental components in processors, digital signal processors, and other computational units. A full adder is a combinational circuit that adds three binary inputs—two significant bits and a carry-in—and generates two outputs: the sum and carry-out. Since adders are extensively used in arithmetic operations, their efficiency has a direct impact on the overall system performance. Conventional CMOS full adder designs typically involve a high transistor count, leading to increased power consumption and propagation delay. To overcome these limitations, hybrid logic techniques are employed, which integrate multiple logic styles to reduce transistor count, enhance speed, and minimize power dissipation. As a result, the design of low-power full adders using hybrid logic has emerged as a significant area of research in VLSI circuit design.

Methodology (Proposed Design)

Conventional Full Adder

A standard full adder has three inputs—A-, B-, and Cin-—and produces two outputs: Sum and Cout. The corresponding logic expressions are: • Sum = A ex-or B ex-or Cin• Cout = AB + B._Cin + A._CinIn conventional CMOS implementations, a high number of transistors is required, which leads to increased power consumption.

B. Hybrid Logic Design The proposed full adder is designed using a hybrid logic approach that integrates multiple logic styles, including:

• Complementary CMOS logic• Pass transistor logic (PTL)• Transmission gate logic By combining these techniques, the design achieves a reduction in transistor count and switching activity, while still preserving proper signal integrity and performance.

C. Circuit Implementation

Simulation results indicate that the proposed hybrid logic full adder offers notable performance enhancements over conventional CMOS designs. The circuit achieves lower power consumption by reducing switching activity and optimizing the use of transistors. Furthermore, the propagation delay is significantly decreased, resulting in improved operating speed.

In addition, the hybrid logic approach reduces the overall circuit area by minimizing the number of transistors required. These advantages make the proposed full adder an efficient choice for low-power, high-speed VLSI applications. The hybrid logic structure also reduces the overall area of the circuit by decreasing the number of required transistors. These improvements make the proposed design suitable for low-power and high-speed VLSI applications.

Conclusion

This paper introduced a low-power CMOS full adder design based on hybrid logic techniques. By integrating various logic styles, the proposed approach successfully minimizes power consumption, propagation delay, and transistor count. Simulation results validate that the hybrid full adder achieves better efficiency than conventional designs. Hence, the proposed architecture is well-suited for use in arithmetic units, digital signal processors, and other VLSI systems that demand low power and high performance.

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