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Study to Identify the Effect of Loop Inductance on the Lightning Impulse Waveform Evaluated Using IEC 60060-1 Ed. 3

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Abstract
Loop Inductance plays a significant role in the generation of lightning impulse waveform. Loop inductance is formed as a part of the impulse generation and measurement circuit including connections, types of front resistors used, self-inductance of the components in the impulse generator including internal connection of the impulse generator. These additional inductances cause unwanted oscillations in the lightning impulse wave, and this has different impact with both load and the source capacitance used. The study aims at identifying the effect of loop inductance with different load and source capacitance and determine the relative overshoot parameter β' using the IEC evaluation as per standard 60060-1 Ed 3. The study can help to identify the usage of correct components during the test of electrical equipment's for basic insulation level using lightning impulse generator. A better understanding on effect of loop inductance can improve the operational efficiency of the generator and time utilization of QA/QC test engineers.

Keywords: Basic Insulation level, Lightning Impulse waveform, Loop Inductance, Relative overshoot,

1. INTRODUCTION

The quality control test of electrical equipment's required to test them to test with lightning impulse for basic insulation level (BIL). These tests are carried according to IEC or IEEE standard throughout the world to ensure a standard quality products that can be installed with reliability and assurance.
The Impulse test circuit consist of DC charging section, source capacitor, triggering circuit, measuring loop and Load capacitors refer Figure 1. The Loop inductance is summation of the total series inductance created due to the self-inductance of all the components used in the circuit. This even includes the inductance of the HV connection cables. Due to the Loop inductance in the circuit oscillations occur in the lightning impulse waveform. These oscillations are again a function of the source and the load capacitance. The study aims at identifying this effect by varying the loop inductance with different source and load capacitance and evaluate the lightning impulse wave according to IEC 60060-1. Ed. 3.

2. RESEARCH METHODOLOGY

The study is done in two case study with three different themes in each case study.

A. CASE STUDY I

The case study one is done to identify the effect of loop inductance with a load capacitance set to a low, medium and high while source capacitance set to a low value. The Loop inductance is varied from 0uH till 100uH in steps of 10uH.

Theme 1: Low Source capacitance low load capacitance. The source capacitance is selected as 100nF, and load capacitance is selected as 680pF.

Theme 2: Low source capacitance medium load capacitance. The source capacitance is selected as 100nF, and load capacitance is selected as 4.7nF.

Theme 3: Low source Inductance high load capacitance. The source capacitance is selected as 100nF, and load capacitance is selected as 10nF.

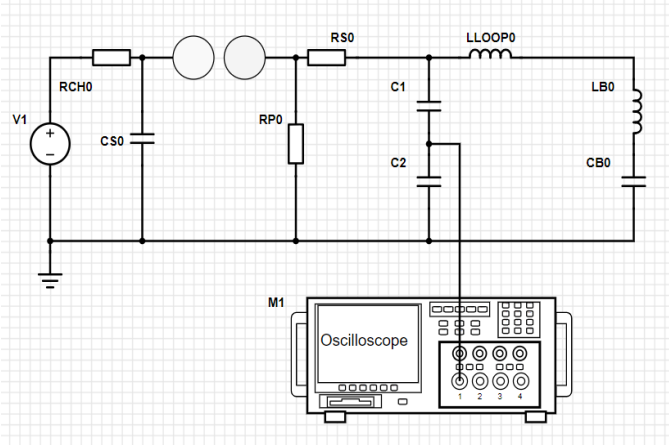


Figure 1: Case study Schematic

V1- DC source, RS0- Series Resistor, RCH0- Charging resistor, RP0-Parallel Resistor, CS0- Source capacitor, C1- Divider Capacitance, LLOOP- Loop Inductance, LB0- Load Inductance, CB0- Load Capacitance

B. CASE STUDY II

The case study two is done to identify the effect of loop inductance with a load capacitance set to a low, medium and high while source capacitance set to a high value.

Theme 4: High Source capacitance low load capacitance. The source capacitance is selected as 1uF, and load capacitance is selected as 680pF.

Theme 5: High source capacitance medium load capacitance. The source capacitance is selected as 1uF, and load capacitance is selected as 4.7nF.

Theme 6: High source Inductance high load capacitance. The source capacitance is selected as 1uF, and load capacitance is selected as 10nF.

For both the case study the schematic used is the same, only the values of the source capacitor and the load capacitors are varied.

3. EXPERIMENTAL SETUP

The experimental setup is done in laboratory condition with the impulse generator as Haefely AG make RSG unit which has variable passive components for resistors, capacitors and inductors. The Digitizer measurement for the evaluation as per IEC 60060-1 ED 3 is using HiAS 744 device and evaluation software.

Figure 2: experimental test setup

4. RESULTS AND TABULATION

The result was collected in the form of waveform and the following parameters such as Upk-Peak Voltage, T1- Front Time, T2- Tail Time, β'- Relative overshoot were tabulated for each Theme separately.

The percentage deviation is calculated from the waveform values with circuit were no loop inductance used as reference. The deviation calculation is done using standard percentage error calculation method. The Percentage error for Upk, T1 and T2 is also tabulated for comparison.

For Case Study I

a. Theme 1: Low Source capacitance low load capacitance.

CS nF	RP Ohm	RS Ohm	LS uH	CL pF	Upk V	UpK % Dev	T1 uS	T1 Dev %	T2 uS	T2 Dev %	Beta'%
100	680	47	0	680	1.159	0.00%	1.298	0.00%	56.397	0.00%	0.91
100	680	47	10	680	1.16	0.09%	1.249	-3.78%	56.261	-0.24%	0.88
100	680	47	20	680	1.161	0.17%	1.199	-7.63%	56.136	-0.46%	0.89
100	680	47	30	680	1.162	0.26%	1.163	-10.40%	56.055	-0.61%	0.89
100	680	47	40	680	1.164	0.43%	1.104	-14.95%	55.943	-0.81%	0.94
100	680	47	50	680	1.165	0.52%	1.051	-19.03%	55.814	-1.03%	1.06
100	680	47	60	680	1.167	0.69%	1.002	-22.80%	55.629	-1.36%	0.96
100	680	47	70	680	1.169	0.86%	0.95835	-26.17%	55.495	-1.60%	1.05
100	680	47	80	680	1.172	1.12%	0.920734	-29.07%	55.284	-1.97%	1.05
100	680	47	90	680	1.175	1.38%	0.891395	-31.33%	55.041	-2.40%	1.3
100	680	47	100	680	1.181	1.90%	0.868742	-33.07%	54.598	-3.19%	1.76

Table 1: Theme 1 measurements

b. Theme 2: Low source capacitance medium load capacitance.

CS nF	RP Ohm	RS Ohm	LS uH	CL pF	Upk V	UpK % Dev	T1 uS	T1 Dev %	T2 uS	T2 Dev %	Beta'%
100	680	100	0	4.7	1.115	0.00%	1.421	0.00%	59.031	0.00%	0.87
100	680	100	10	4.7	1.125	0.90%	1.156	-18.65%	58.071	-1.63%	1.24
100	680	100	20	4.7	1.153	3.41%	1.074	-24.42%	58.988	-0.07%	3.56
100	680	100	30	4.7	1.18	5.83%	1.087	-23.50%	53.963	-8.59%	6.14

100	680	100	40	4.7	1.226	9.96%	1.153	-18.86%	50.758	-14.01%	9.88
100	680	100	50	4.7	1.262	13.18%	1.222	-14.00%	48.298	-18.18%	12.43
100	680	100	60	4.7	1.297	16.32%	1.316	-7.39%	46.104	-21.90%	14.64
100	680	100	70	4.7	1.325	18.83%	1.383	-2.67%	44.285	-24.98%	16.28
100	680	100	80	4.7	1.352	21.26%	1.447	1.83%	42.552	-27.92%	17.72
100	680	100	90	4.7	1.376	23.41%	1.512	6.40%	41.115	-30.35%	19.00
100	680	100	100	4.7	1.402	25.74%	1.584	11.47%	39.574	-32.96%	20.15

Table 2: Theme 2 measurements

c. Theme 3: Low source Inductance high load capacitance.

CS nF	RP Ohm	RS Ohm	LS uH	CL pF	Upk V	UpK % Dev	T1 uS	T1 Dev %	T2 uS	T2 Dev %	Beta'%
100	470	47	0	10	1.061	0.00%	1.203	0.00%	42.571	0.00%	0.84
100	470	47	10	10	1.129	6.41%	0.99548	-17.25%	38.694	-9.11%	6.8
100	470	47	20	10	1.215	14.51%	1.145	-4.82%	34.281	-19.47%	13.37
100	470	47	30	10	1.264	19.13%	1.259	4.66%	31.926	-25.01%	16.44
100	470	47	40	10	1.326	24.98%	1.421	18.12%	29.087	-31.67%	19.51
100	470	47	50	10	1.367	28.84%	1.549	28.76%	27.208	-36.09%	21.27
100	470	47	60	10	1.404	32.33%	1.681	39.73%	25.68	-39.68%	22.53
100	470	47	70	10	1.433	35.06%	1.791	48.88%	24.463	-42.54%	23.47
100	470	47	80	10	1.458	37.42%	1.886	56.77%	23.433	-44.96%	24.11
100	470	47	90	10	1.481	39.59%	1.976	64.26%	22.475	-47.21%	24.42
100	470	47	100	10	1.503	41.66%	2.078	72.73%	21.611	-49.24%	24.46

Table 3: Theme 3 measurements

For Case Study II

d. Theme 4: High Source capacitance low load capacitance.

CS uF	RP Ohm	RS Ohm	LS uH	CL pF	Upk V	UpK % Dev	T1 uS	T1 Dev %	T2 uS	T2 Dev %	Beta'%
1	68	470	0	680	1.03	0.00%	1.332	0.00%	49.449	0.00%	0.5
1	68	470	10	680	1.031	0.10%	1.284	-3.60%	49.343	-0.21%	0.53
1	68	470	20	680	1.032	0.19%	1.237	-7.13%	49.239	-0.42%	0.72

1	68	470	30	680	1.033	0.29%	1.201	-9.83%	49.221	-0.46%	0.55
1	68	470	40	680	1.034	0.39%	1.14	-14.41%	49.085	-0.74%	0.47
1	68	470	50	680	1.034	0.39%	1.089	-18.24%	48.979	-0.95%	0.45
1	68	470	60	680	1.037	0.68%	1.039	-22.00%	48.85	-1.21%	0.5
1	68	470	70	680	1.038	0.78%	0.99347	-25.42%	48.701	-1.51%	0.51
1	68	470	80	680	1.04	0.97%	0.95244	-28.50%	48.582	-1.75%	0.51
1	68	470	90	680	1.043	1.26%	0.922303	-30.76%	48.338	-2.25%	0.76
1	68	470	100	680	1.048	1.75%	0.898448	-32.55%	48.052	-2.83%	1.01

Table 4: Theme 4 measurements

e. Theme 5: High source capacitance medium load capacitance.

CS uF	RP Ohm	RS Ohm	LS uH	CL pF	Upk V	UpK % Dev	T1 uS	T1 Dev %	T2 uS	T2 Dev %	Beta' %
1	68	100	0	4.7	1.023	0.00%	1.488	0.00%	49.924	0.00%	0.57
1	68	100	10	4.7	1.033	0.98%	1.224	-17.74%	49.087	-1.68%	0.83
1	68	100	20	4.7	1.056	3.23%	1.128	-24.19%	47.534	-4.79%	2.78
1	68	100	30	4.7	1.081	5.67%	1.134	-23.79%	45.898	-8.06%	5.33
1	68	100	40	4.7	1.122	9.68%	1.196	-19.62%	43.346	-13.18%	8.91
1	68	100	50	4.7	1.154	12.81%	1.265	-14.99%	41.407	-17.06%	11.35
1	68	100	60	4.7	1.184	15.74%	1.337	-10.15%	39.686	-20.51%	13.55
1	68	100	70	4.7	1.21	18.28%	1.407	-5.44%	38.189	-23.51%	15.14
1	68	100	80	4.7	1.235	20.72%	1.474	-0.94%	36.821	-26.25%	16.66
1	68	100	90	4.7	1.257	22.87%	1.547	3.97%	35.624	-28.64%	17.81
1	68	100	100	4.7	1.28	25.12%	1.622	9.01%	34.362	-31.17%	19.09

Table 5: Theme 5 measurements

f. Theme 6: High source Inductance high load capacitance.

CS uF	RP Ohm	RS Ohm	LS uH	CL pF	Upk V	UpK % Dev	T1 uS	T1 Dev %	T2 uS	T2 Dev %	Beta' %
1	68	47	0	10	1.022	0.00%	1.339	0.00%	49.799	0.00%	0.54
1	68	47	10	10	1.078	5.48%	1.083	0.00%	45.921	0.00%	5.53
1	68	47	20	10	1.159	13.41%	1.224	13.02%	40.968	-10.79%	12.23

1	68	47	30	10	1.205	17.91%	1.335	23.27%	38.29	-16.62%	15.36
1	68	47	40	10	1.265	23.78%	1.515	39.89%	34.998	-23.79%	18.76
1	68	47	50	10	1.306	27.79%	1.648	52.17%	32.803	-28.57%	20.62
1	68	47	60	10	1.340	31.12%	1.773	63.71%	30.998	-32.50%	22.01
1	68	47	70	10	1.367	33.76%	1.883	73.87%	29.643	-35.45%	22.85
1	68	47	80	10	1.393	36.30%	1.99	83.75%	28.329	-38.31%	23.91
1	68	47	90	10	1.415	38.45%	2.095	93.44%	27.236	-40.69%	24.48
1	68	47	100	10	1.437	40.61%	2.213	104.34%	26.213	-42.92%	24.81

Table 6: Theme 6 measurements

5. DATA ANALYSIS

From the collected primary data, a detailed analysis was conducted to identify the relation of Loop inductance with the change in the source and the load capacitance.

Analysis on Case Study I

Theme 1: From the collected data, with a low load capacitance and low source capacitance the Upk value variation from no loop inductance till 100uH loop inductance is less that 2%, But T1 is gradually decreasing to 33% and with a marginal variation of T2 of 3.2% after introduction of 100uH loop inductance. Relative overshoot measured was less than 2% even though the T1 has deviated extensively.

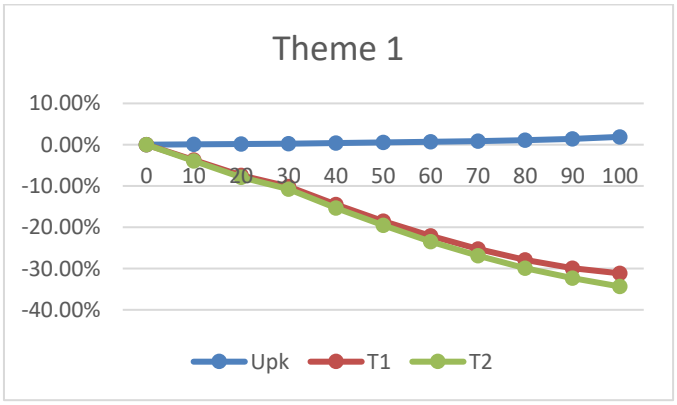


Figure 3: Theme 1 trendline for deviation in Upk, T1 and T2 with respect to Loop Inductance

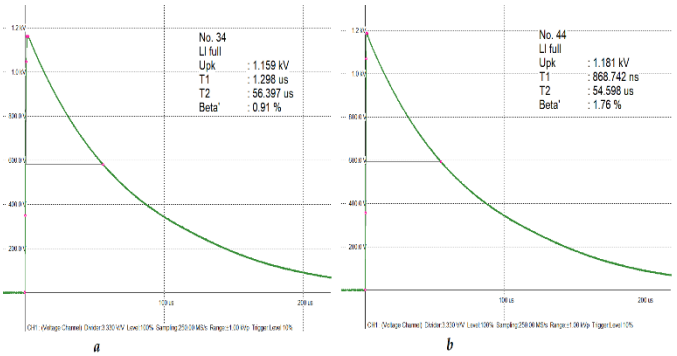


Figure 4: Theme 1 waveform for; a- No loop inductance, b- 100uH loop inductance

Theme 2: From table 2, with a low Source capacitance and Medium Load capacitance, the Upk value vary till 25.74% ,with T1 deviating in the negative quadrant with increasing trend till 20uH at -24.42% and then

following a decreasing trend till 70uH at -2.67% and then following a increasing trend in the positive quadrat till 11.47% at 100uH inductance. A drastic change in the T2 occurred with maximum deviation of 32.96% in the negative quadrant with introduction of 100uH.

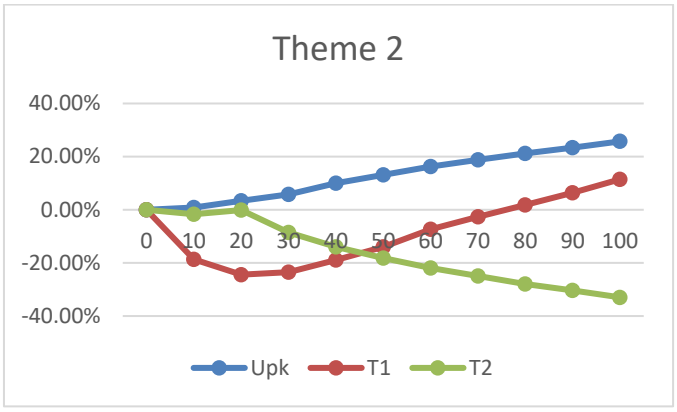


Figure 5: Theme 2 trendline for deviation in Upk, T1 and T2 with respect to loop inductance.

Introduction of high loop inductance has increased the oscillation in the circuit causing an increased front time T1 and reduced tail time T2. This oscillation also increased the output peak voltage with a higher relative overshoot.

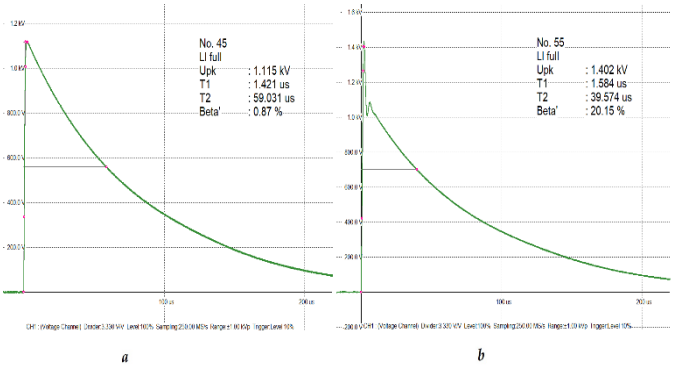


Figure 6: Theme 2 waveform for; a- No loop inductance, b- 100uH loop inductance

Theme 3: From table 3, with a low source capacitance and high load capacitance, the Upk value vary till 41.66%, with T1 deviating in the negative quadrant with decreasing trend till starting from -17.25 at 10uH inductance to -4.82% at 20uH,Then moving to positive quadrant in increasing trend till 72,73% with 100uH inductance. T2 deviation trend in the negative quadrant in increasing manner till 49.24% with 100uH inductance.

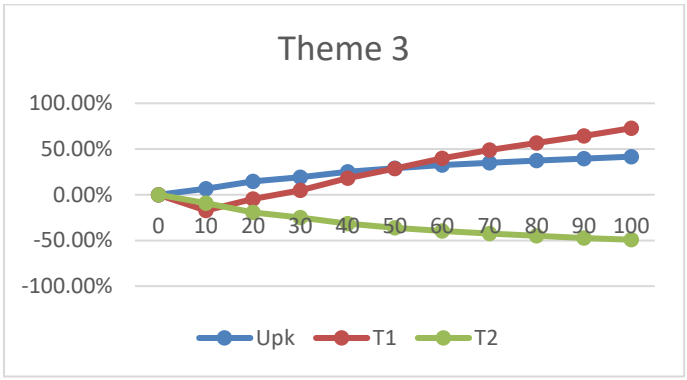


Figure 7: Theme 3 trendline for deviation in Upk, T1 and T2 with respect to loop inductance.

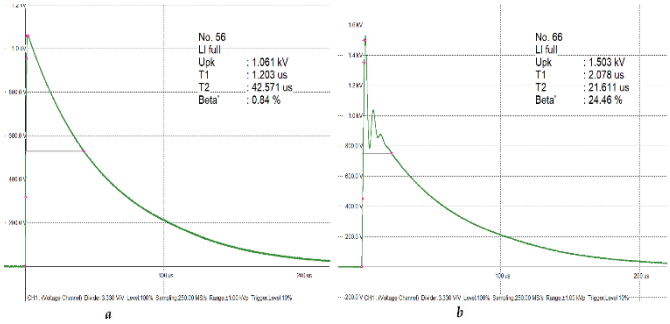


Figure 8: Theme 3 waveform for; a- No Loop Inductance, b- 100uH loop inductance

Analysis on Case Study II

Theme 4: Data from table 4 shows that there is no significant change in the Upk value and the maximum deviation is 1.75% at 100uH inductance. The T1 value has very high deviation trending in the negative quadrant till 32.55% with 100uH inductance. The T2 deviation is slightly in the negative quadrant till -2.83% in the 100uH loop inductance.

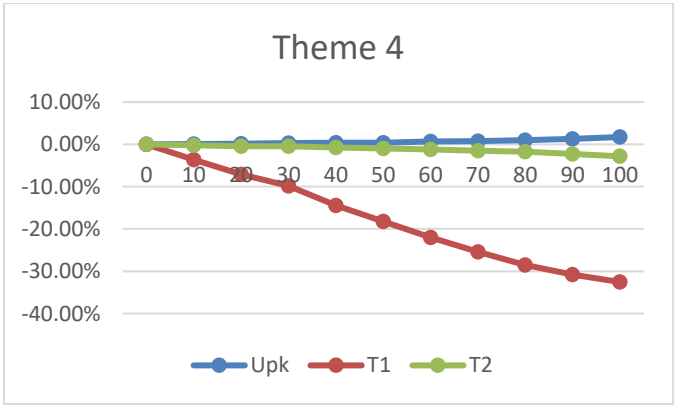


Figure 9: Theme 4 trendline for deviation in Upk, T1 and T2 with respect to loop inductance.

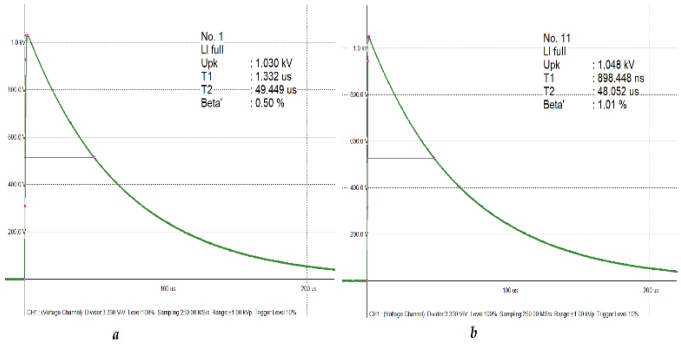


Figure 10: Theme 4 waveform for; a- No Loop Inductance, b- 100uH loop inductance

Theme 5: Data from table 5 shows that there is significant change in the Upk value, and the maximum deviation is 25.12% with 100uH inductance. T1 time is deviating in the negative quadrant with decreasing trend till 80uH at -0.94% and then following a positive trend till 100uH inductance with value of 9.01% . The T2 deviation is in the increasing trend in negative quadrant till -31.17% with 100uH loop inductance. The relative overshoot is increased to 19.09%.

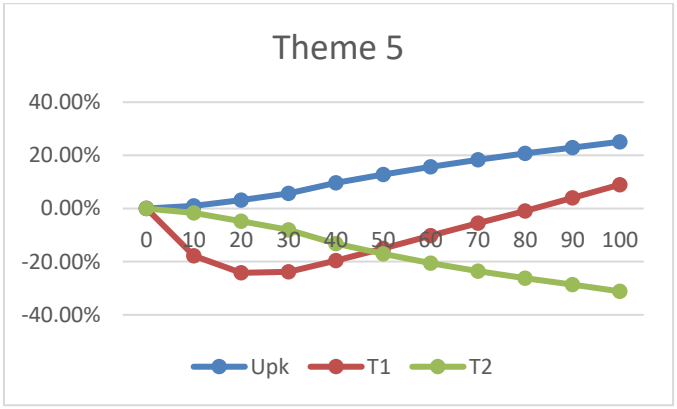


Figure 11: Theme 5 trendline for deviation in Upk, T1 and T2 with respect to loop inductance.

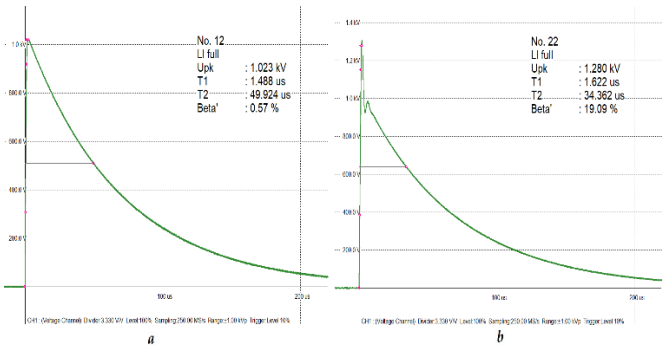


Figure 12: Theme 5 waveform for; a- No Loop Inductance, b- 100uH loop inductance

Theme 6: Table 6 provide data showing that there is significant change in the Upk value, and the maximum deviation is 40.61% with 100uH inductance. T1 time deviation is large in this case with maximum deviation with 100uH inductance noted 104.34%. The T2 deviation is in the increasing trend in negative quadrant till -42.92% with 100uH loop inductance.

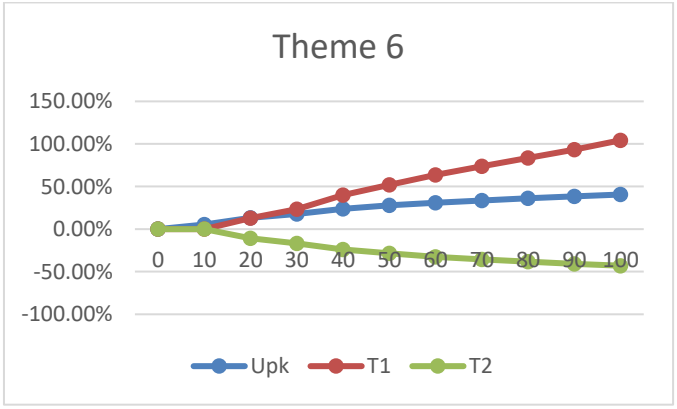
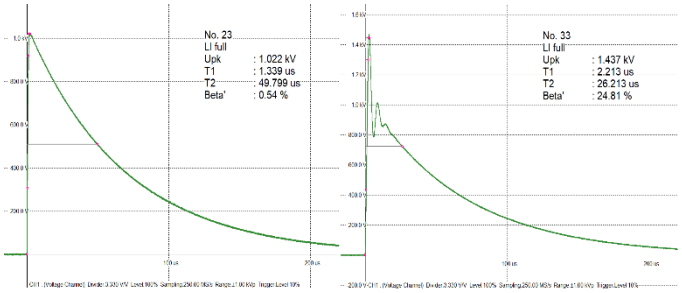


Figure 13: Theme 6 trendline for deviation in Upk, T1 and T2 with respect to loop inductance.



a *b*

Figure 14: Theme 6 waveform for; a- No Loop Inductance, b- 100uH loop inductance

6. CONCLUSION

From Case study 1, with small source capacitor selected, it is evident that the loop inductance play a vital role when the load rages are in medium and high range. There are no significant deviations in Upk, T1 and T2 with the small load. Similarly with case study II having large source capacitor selected, it is observed that the low range capacitance of the load is not having significant change with the impulse parameters, but the medium and large load capacitors range have a very significant effect on the loop inductance. It is observed with the results that with increase in loop inductance, in higher load range, very high oscillation observed on the wavefront and theses oscillations causing a very high relative overshoot. So, it is recommended to reduce the loop inductance in the circuit while doing lightning impulse testing. To reduce the loop inductance, generally, the parts used in the circuit should be of very small self-inductance. Some of the methods to achieve this is to shorten the distance between the test object and the Impulse generator. Also using long inductance wide copper foil as high voltage connections instead of wires.

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