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Domino Logic Approach For 8 Bit Comparator Design

P. C. Praveen Kumar[1], Mohammed Zain[2], B. Sivakumar Naik[3], P. Mokshith Rao[4]

[1,2,3,4]Department of ECE, G. Pulla Reddy Engineering College (Autonomous): Kurnool,Andhra Pradesh,India

Abstract

Digital comparators are widely used in digital systems for tasks requiring data comparison. Conventional comparators designed using technologies such as CMOS provide the necessary speed and accuracy required by comparator applications. However, these comparators often face limitations and trade-offs between speed and power efficiency, especially in high-frequency applications due to their complex static design. This results in higher energy consumption and reduced operational efficiency, especially in low-power and high-frequency environments. To address these limitations, this paper explores a domino CMOS logic approach to design an 8-bit comparator that reduces power consumption. This project aims to provide an alternative to conventional CMOS comparators in high-performance VLSI circuits.

Keywords: Domino Logic, Comparator, CMOS

1. INTRODUCTION

Comparators play a crucial role in various digital applications, including arithmetic units, memory address decoding, signal processing, and high-speed communication systems. Traditional CMOS-based comparators often suffer from increased delay and power dissipation due to their complex static design. This makes them less efficient in high-frequency and low-power applications, where speed and energy efficiency are critical design constraints.

One approach to addressing these challenges is the use of domino logic, a form of dynamic CMOS logic that enhances circuit performance. Domino logic operates through a precharge and evaluation mechanism, reducing transistor count and minimizing power dissipation compared to static CMOS designs. Its ability to achieve high-speed operation with lower power makes it a suitable choice for implementing efficient comparators in VLSI circuits.

This paper presents the design and implementation of an 8-bit comparator using domino logic. The rest of the paper is organized as follows: Section II (A) discusses the fundamentals of comparator design and the limitations of static CMOS comparators. Section II (B) introduces the proposed domino logic-based 8-bit comparator architecture. Section III presents the simulation results. Section IV presents performance analysis, while Section V concludes the paper.

2. Comparator design

This section describes the working of domino logic and followed by the design methodology of the comparator.

A. Domino Logic

Domino logic is a part of the dynamic CMOS family of circuits, the designs of which are clocked and synchronized. As such, the operation of a domino logic circuit is entirely reliant on the clock signals. A domino logic circuit typically consists of two parts: A pull down network (PDN) made and connected together with NMOS depending on the required logic and two clocked MOS transistors. Clocked PMOS is positioned between the supply and PDN while the clocked NMOS is positioned between the PDN and ground. A domino logic circuit has two operation phases: Precharge and Evaluation phase. Both phases together constitute the operation of the complete circuit in synchronization with the clock.

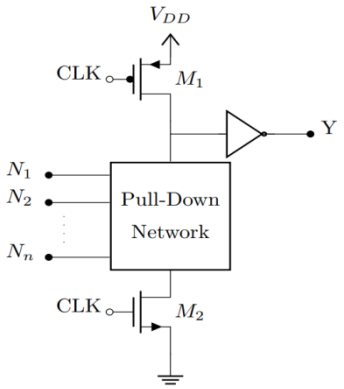

Fig 1. General Domino Logic Implementation

The operation of Domino logic circuits is completely based on the charging and discharging of the MOS capacitance. During the precharge phase (when the clock signal is low), the PMOS precharge transistor is active, charging the output node to a high logic level. Simultaneously, the NMOS evaluation transistor is turned off, ensuring that no discharge occurs. This phase prepares the circuit for evaluation by preloading the output with a defined value. In the evaluation phase (when the clock signal is high), the PMOS precharge transistor turns off, and the NMOS evaluation transistor becomes active. If the pull-down network (PDN) forms a conducting path to the ground, the output discharges to a low logic level. Otherwise, the output remains high. Since there is no static pull-up path, domino logic inherently implements only non-inverting functions and hence requires additional circuitry if an inverting logic operation is needed.

One of the primary advantages of domino logic is its higher switching speed compared to conventional static CMOS designs. This is due to the reduced input capacitance, which results in faster transitions and lower propagation delay. Additionally, the elimination of direct paths between the supply and ground during operation contributes to lower dynamic power dissipation. These characteristics make domino logic well-suited for high-speed, low-power applications.

B. Proposed Architecture of 8-bit comparator

The proposed 8-bit comparator is designed using a hierarchical approach, where instances of 1-bit and 4-

bit comparators are combined to achieve an efficient structure. This implementation requires multiple logic gates and sub components which were all designed using standard domino logic.

At the core of the architecture, a 1-bit comparator serves as the fundamental building block. By combining multiple 1-bit comparators, a 4-bit comparator is constructed to compare larger segments of input data as shown in Fig 2. Finally, two 4-bit comparators are instantiated to form the complete 8-bit comparator. Each stage of the comparator design requires specific clock signals to achieve the desired synchronization of components. Clock signals with different pulse widths are provided to the various stages of the architecture. A linear flow of data and intermediate results is achieved by cascading the different stages.

A simple 1-bit comparator uses one clock signal which is common to all logic gates within it. Thus, the first stage of 4-bit comaparator uses one clock signal. The second stage covers all cases where the values of the outputs G (Greater), E (Equal) and L (Low) are either low logic level or high logic level and since this can be done in parallel, a single clock signal is shared among all the AND gates. The third stage combines specific cases where G and L can be high logic level. This is done using OR gates which also operate in parallel since outputs G, E and L are independent of each other. Thus, the 4-bit comparator requires three clock signals as outputs of subsequent stages are dependent on previous stages.

The proposed architecture of 8-bit comparator uses two 4-bit comparators as shown in Fig 3. These two together form the first stage of the 8-bit comparator. Inputs to these comparators are two byte-long numbers. One comparator performs comparison of higher order nibbles of the byte-long inputs while the other performs lower order nibble comparison. Since the 4-bit comparators operate in parallel, three common clock signals are sufficient for the first stage. The second stage logically checks for all possible cases for each output G, E and L. The second stage uses AND gates and thus a single clock signal is sufficient for the second stage. The third stage combines outputs from the second stage to directly enable or disable G and L. This is done using OR gates and a single clock signal is used. Thus, five clock signals are required to fully compute the three outputs of the three outputs of the 8-bit comparator.

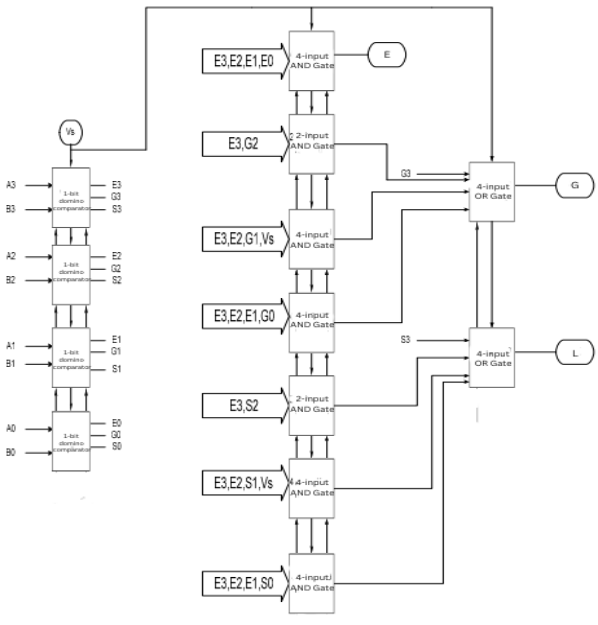

Fig 2. 4-bit comparator architecture

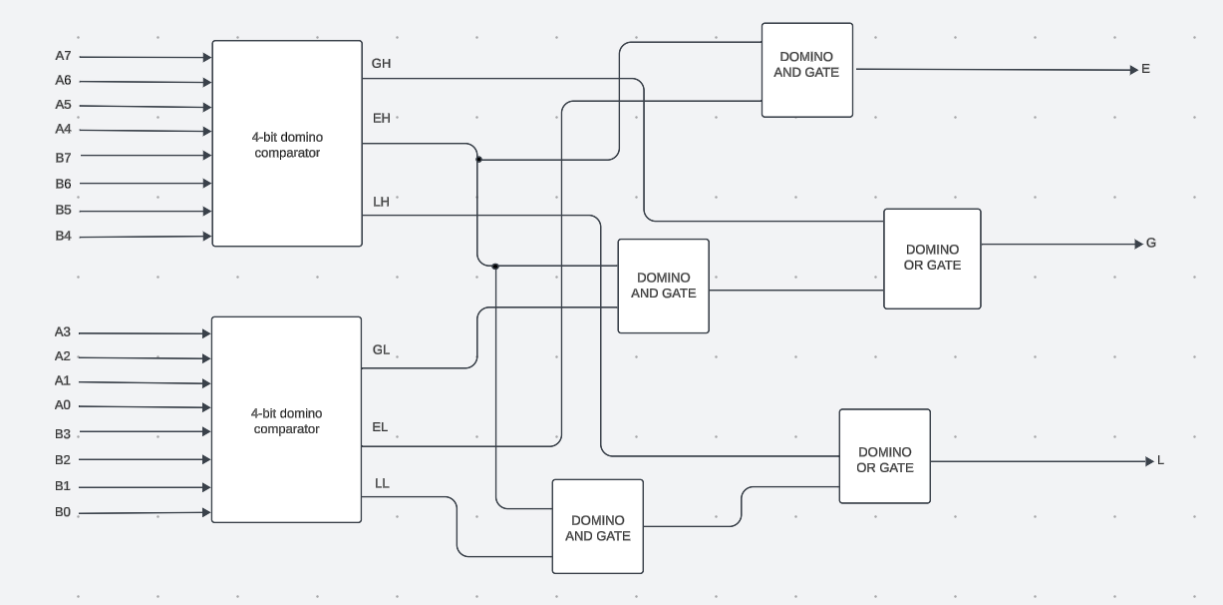

Fig 3. 8-bit comparator architecture

3. SIMULATION RESULTS

The design and simulation of the project was done in Cadence Virtuoso software. A schematic of every logic gate and component was developed and integrated into the final schematic of the 8-bit comparator. Fig 5. shows the final waveform of the designed 8-bit comparator.

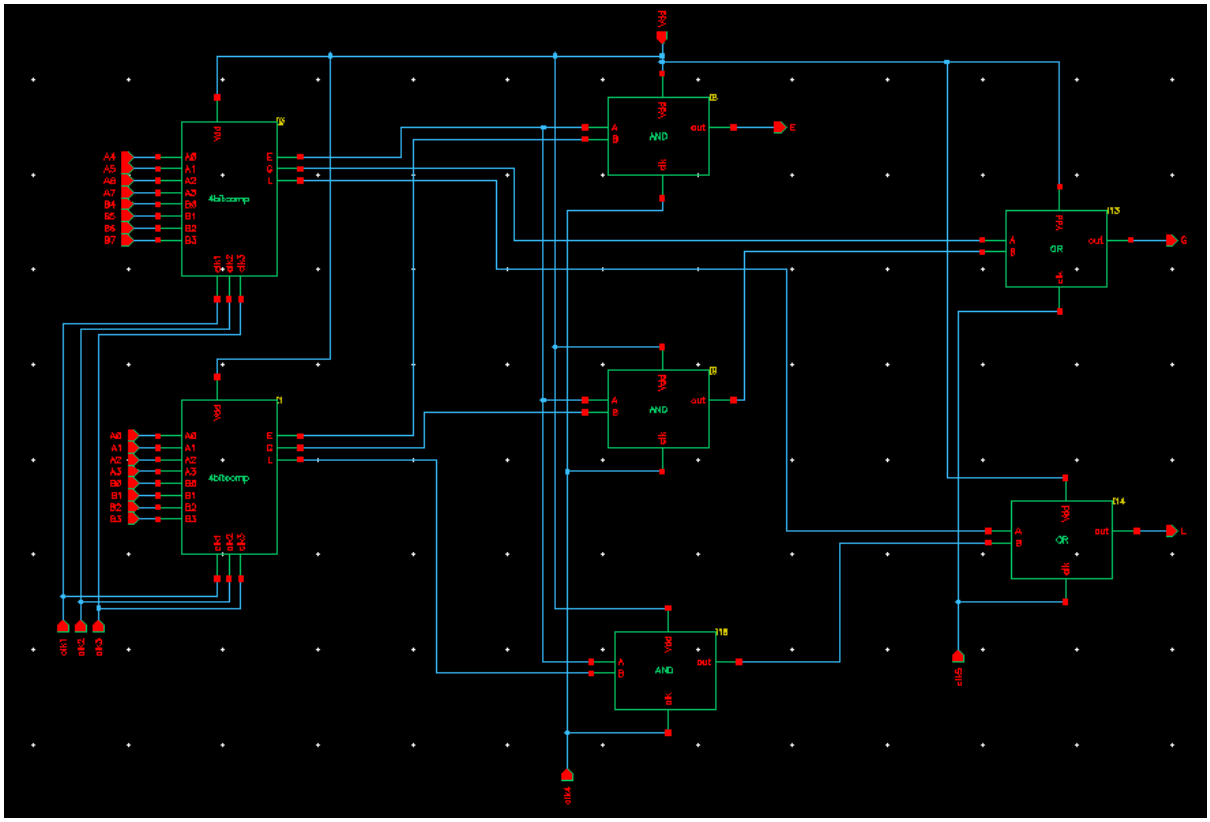

Fig 4. 8-bit comparator schematic

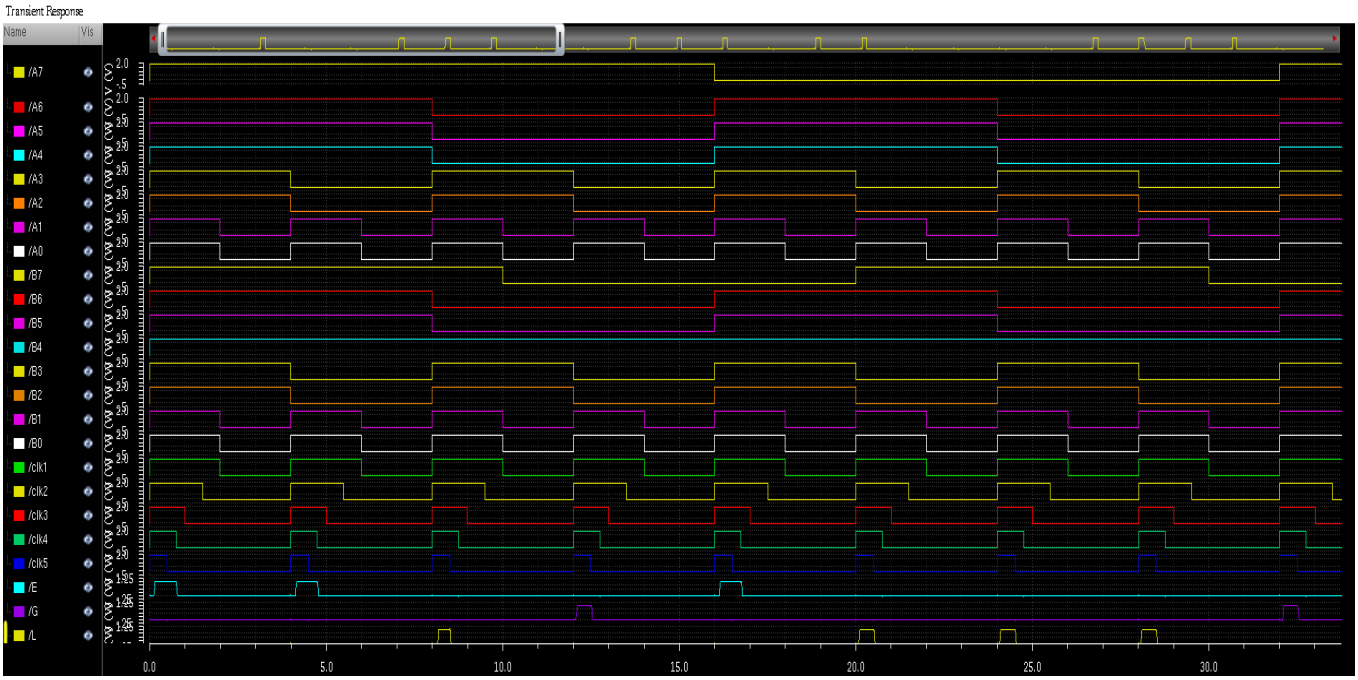

Fig 5. 8-bit comparator waveform

The five clock signals provided to the comparator can also be seen in the waveform. These clock signals have the same period but differ in the size of the pulse width The outputs G, E and L only appear during the evaluation phase (when final stage clock is logic high). Keeper transistors were also included in the design of the components of the comparator which results in reduced noise in the output waveform. The circuit functions satisfactorily as indicated by the waveform.

4. COMPARATIVE ANALYSIS

The 8-bit comparator was designed using 90nm technology. A comparison between design using CMOS and domino logic is done.

Table: Power and Delay

Type of Logic	Parameters		
	Reference Frequency	Power (uW)	Delay (ns)
8-bit domino comparator	250MHz	122.25	0.058
8-bit CMOS comparator	250MHz	204.12	0.02

From the table, it can be observed that the 8-bit domino comparator works efficiently by utilizing nearly 40% less power when compared to the equivalent CMOS design. The CMOS comparator is relatively faster with a slightly lower delay. The CMOS comparator works faster with lower delay and is better suited for very high speed operations with a trade-off between speed and power. The domino comparator is more optimal as it reduces a large amount of power with a slight reduction in speed of operation.

5. Conclusion

The research explores the design of an 8-bit comparator using domino logic, highlighting its advantages

over conventional CMOS in terms of power efficiency. By structuring the comparator hierarchically with 4-bit modules and utilizing multiple clock signals for synchronization, the design ensures accurate operation. Simulations confirm its correctness, and comparisons with CMOS at 90nm technology show a 40% reduction in power consumption. The findings suggest that domino logic is a promising approach for optimizing comparator performance in low-power VLSI applications.

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