International Journal for Multidisciplinary Research (IJFMR)
E-ISSN: 2582-2160 ● Website: www.ijfmr.com ● Email: editor@ijfmr.com

Design and Implementation of SRAM Using FinFET

Aaditri Singh[1], Kavyansh Saxena[2], Ms. Kanika Jindal[3]

[1,2,3]Electronics and Communication Engineering, Noida Institute of Engineering and Technology, Greater Noida, Uttar Pradesh

Abstract

With the continuous scaling of CMOS technology, traditional SRAM designs face challenges such as increased leakage current, reduced reliability, and higher power consumption. FinFET (Fin Field-Effect Transistor) technology has emerged as a promising alternative due to its superior electrostatic control, reduced leakage, and enhanced performance. This paper explores the implementation of SRAM using FinFET technology, analyzing its advantages over conventional bulk CMOS-based SRAM. We investigate key design considerations, including read/write stability, power efficiency, and performance metrics in different FinFET-based SRAM topologies. Simulation results demonstrate that FinFET SRAM exhibits lower leakage power, improved noise margins, and better scalability compared to traditional SRAM designs. Additionally, the impact of various process variations on FinFET SRAM performance is analyzed to assess its robustness in nanoscale circuits. The findings highlight FinFET's potential to drive the next generation of low-power and high-performance memory architectures.

Keywords: SRAM, FinFET, low-power memory, leakage reduction, nanoscale circuits, performance analysis

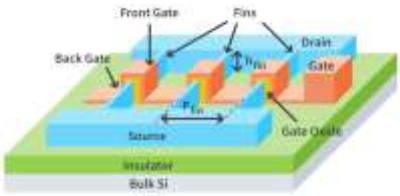

Figure 1 : FinFET Design

I. Introduction

Static Random-Access Memory (SRAM) is a crucial component in modern digital systems, widely used in cache memories, embedded systems, and high-performance computing. As technology scales down to nanometer regimes, conventional bulk CMOS-based SRAM designs face significant challenges, including increased leakage current, short-channel effects, and higher power consumption.

Fin Field-Effect Transistor (FinFET) technology has emerged as a promising solution to overcome these challenges. FinFETs offer superior electrostatic control, reduced leakage, and improved performance due to their three-dimensional structure, which enhances gate control over the channel. These

characteristics make FinFETs particularly suitable for SRAM design, enabling lower power consumption, better stability, and enhanced scalability compared to traditional CMOS SRAM cells.

This paper presents an in-depth analysis of SRAM implementation using FinFET technology. It explores various SRAM cell topologies, focusing on their power efficiency, read/write stability, and robustness under process variations. Through comparative analysis and simulation results, we evaluate the advantages of FinFET-based SRAM over conventional designs. The study aims to highlight how FinFET technology can drive the next generation of energy-efficient and high-performance memory architectures, addressing the growing demands of modern computing systems.

II. EASE OF USE

The implementation of SRAM using FinFET technology offers significant improvements in performance and power efficiency while maintaining a feasible level of design complexity. FinFET-based SRAM circuits are compatible with existing CMOS fabrication processes, making their integration into modern semiconductor workflows relatively straightforward. Compared to traditional bulk CMOS SRAM, FinFET-based designs exhibit better scalability, reducing design constraints associated with leakage currents and short-channel effects. These advantages contribute to ease of adoption in advanced memory architectures.

Moreover, the improved electrostatic control and reduced variability in FinFET devices simplify design considerations for SRAM stability and reliability. Design tools and simulation frameworks widely support FinFET modeling, enabling efficient optimization of SRAM structures without requiring extensive modifications to existing methodologies. While initial adaptation may require adjustments in layout and manufacturing processes, the long-term benefits in power efficiency and performance make FinFET-based SRAM an accessible and practical choice for next-generation memory solutions.

III. DESIGN OF 6T SRAM USING FINFET

The six-transistor (6T) SRAM cell is an essential component in digital memory systems due to its speed and reliability, making it a preferred choice for cache memory. This memory cell consists of six transistors arranged in a flip-flop structure, specifically configured with two access transistors and cross-coupled inverters. The storage nodes, formed by cross-coupled inverters, hold the data, with each inverter consisting of a PMOS and an NMOS transistor connected in series.

These transistors are linked gate-to-gate and drain-to-drain to facilitate data storage. The access transistors enable reading and writing operations by connecting each storage node to one of the bitlines (BL). During a read operation, the wordline (WL) activates the access transistors, allowing the stored data to be read from the SRAM cell. For write operations, the bitline is driven to the required value, and the wordline is activated to change the state of the storage nodes accordingly.

Advantages of 6T SRAM Cell:

- High-speed operation enables fast read and write access, making it ideal for cache memory.
- Cross-coupled inverter structure ensures stable data retention without requiring periodic refreshing, unlike DRAM.
- Lower power consumption compared to DRAM due to the absence of refresh cycles.
- Reduced leakage current compared to other SRAM designs.
- Limitations of 6T SRAM Cell:
- Larger area requirement per cell compared to alternative memory designs like 4T or 1T DRAM cells.

- Increased design complexity due to the need for two cross-coupled inverters and two access transistors.
- Potential data disturbance during read operations, which may lead to errors if not managed properly.
- Role of Conventional 6T SRAM in Modern Circuits:
- Essential for cache memory applications due to its speed, stability, and energy efficiency.
- Consumes more area per bit compared to alternative memory architectures.
- Higher power consumption during read and write operations than DRAM.
- Trade-offs must be made between SRAM's stability and DRAM's higher density.
- Chip designers must carefully evaluate these factors when selecting memory solutions

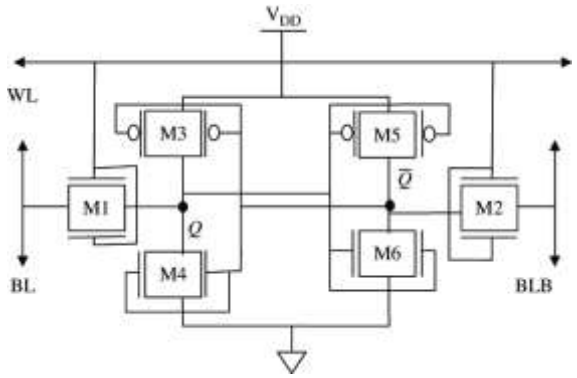

Figure 2 : FINFET based SRAM 6T cell [1]

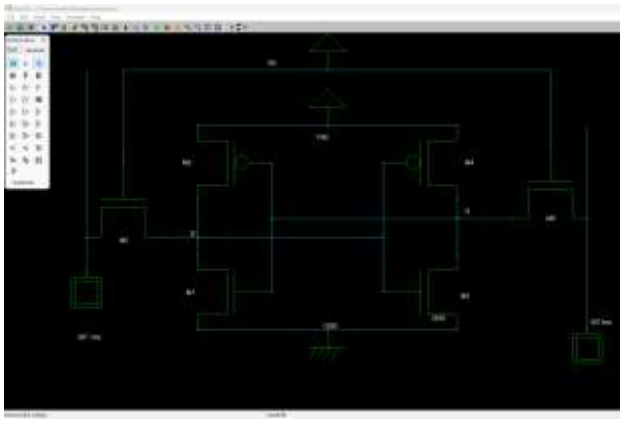

Figure 3 : Conventional FINFET based SRAM 6T cell

Figures 2 and figure 3 illustrate the proposed FinFET-based 6T SRAM cell and its layout. FinFET technology, a three-dimensional transistor design, provides notable advantages over conventional planar transistors in terms of performance and power efficiency. When applied to 6T SRAM cell design, FinFET technology improves multiple aspects of memory cell functionality, including reduced leakage current and enhanced power optimization. However, despite these advantages, FinFET-based designs introduce additional challenges, such as increased manufacturing complexity and design optimization requirements. Engineers must carefully refine the layout and structure of the 6T SRAM cell to fully utilize the benefits of FinFET technology while mitigating its potential limitations.

IV. DESIGN METHODOLGY

The design methodology for implementing SRAM using FinFET technology involves a structured approach that ensures optimal performance, power efficiency, and stability. The process begins with the selection of a suitable FinFET-based SRAM cell topology, such as the conventional 6T, 8T, or 10T SRAM architectures. These topologies are analyzed based on key performance metrics, including read/write stability, leakage power, and noise margins.

Following the topology selection, transistor-level circuit design is carried out using FinFET models compatible with modern semiconductor process nodes. The FinFET devices are designed with appropriate gate lengths, fin heights, and doping profiles to achieve better electrostatic control and reduced leakage currents. Next, schematic simulations are performed using industry-standard electronic design automation (EDA) tools such as Cadence Virtuoso, HSPICE, or Synopsys TCAD. These simulations help evaluate the cell's static noise margin (SNM), read/write delays, and overall power consumption.

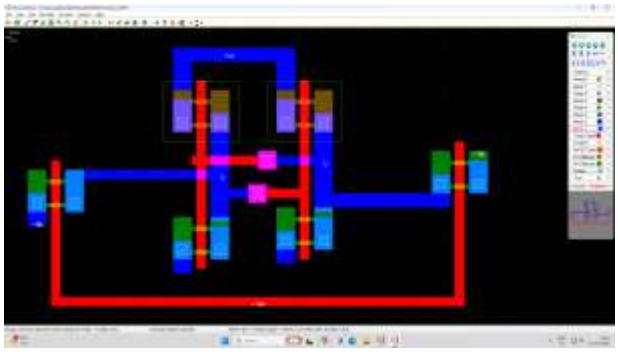

Figure 4 : Layout of CMOS based SRAM 6T cell in 12nm

After validating the circuit performance, the layout design is implemented using FinFET-compatible process design kits (PDKs). Layout-dependent effects such as parasitic capacitance and resistance are considered to optimize the physical design. The final step involves post-layout simulations to verify the impact of fabrication constraints, process variations, and environmental factors on the SRAM cell's functionality and reliability. The results are compared with conventional CMOS-based SRAM designs to highlight the advantages of FinFET technology in terms of power efficiency, stability, and scalability.

V. RESULT ANALYSIS

When designing a 6T SRAM cell using FinFET technology instead of conventional CMOS, several enhancements and advantages can be achieved. The power consumption during SRAM read and write operations depends on factors such as supply voltage, clock frequency, access patterns, and the specific cell architecture. Read operations primarily consume power due to the internal circuitry required for data retrieval, while write operations demand more power as they involve charging or discharging the storage nodes, leading to transistor state changes. Minimizing power consumption is crucial, particularly in battery-operated devices, where efficient power management extends battery life. To achieve this, design strategies such as optimizing cell architecture, employing low-power circuit techniques, and implementing advanced power management methods are utilized.

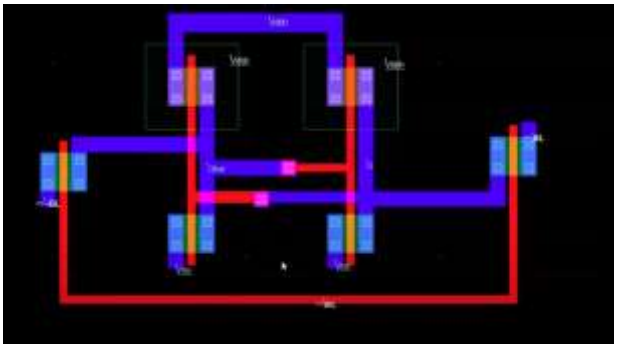

Figure 6 :Analysis of CMOS based SRAM 6T cell in 12nm

Power Efficiency Improvements: FinFET technology generally exhibits lower leakage currents than CMOS, significantly reducing static power consumption in 6T SRAM cells. This enhanced efficiency is particularly beneficial in standby modes, where power conservation is critical. Additionally, FinFETs offer improved switching speeds, resulting in faster read and write operations, which in turn lowers access times and enhances overall memory performance.

Scalability and Stability: The ability of FinFET technology to scale down to smaller feature sizes enables higher memory cell density on a chip. Moreover, its superior control over current flow enhances stability in the 6T SRAM cell, helping to mitigate common issues such as read disturbances, write instability, and other reliability challenges.

Area and Performance Efficiency: Although FinFET technology introduces a slightly more complex manufacturing process, it provides better area efficiency than planar CMOS, leading to smaller memory cell sizes and overall chip area reduction. The combination of improved power efficiency and faster switching speeds results in a higher performance-per-watt ratio, meaning that FinFET-based 6T SRAM cells can achieve superior performance levels while consuming less power compared to CMOS-based designs.

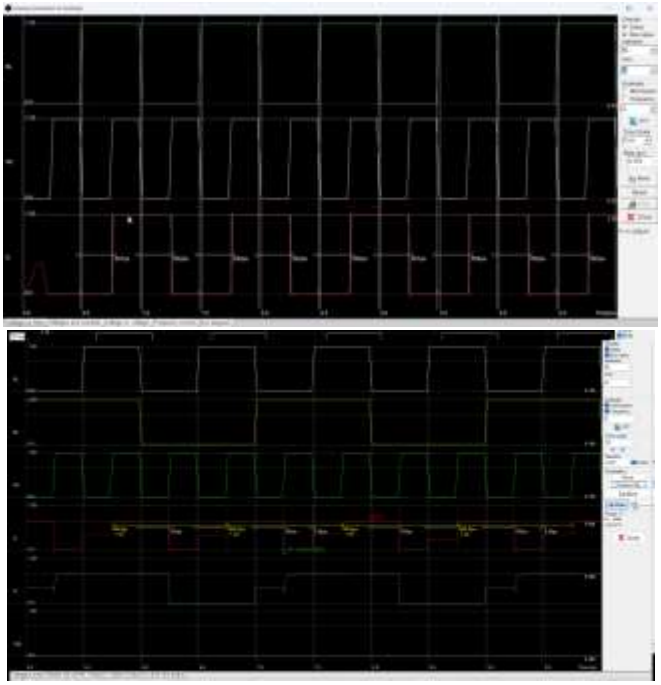

Figure 7: Analysis of FINFET based SRAM 6T cell in 14nm

CONCLUSION

The implementation of SRAM using FinFET technology provides an effective solution to the limitations of traditional CMOS-based memory designs. With superior electrostatic control, reduced leakage power, and enhanced performance, FinFET-based SRAM is well-suited for next-generation low-power and high-speed memory applications. This study demonstrates that FinFET SRAM offers improved read/write stability, better noise margins, and greater scalability, addressing key challenges in modern semiconductor design. Additionally, the impact of process variations on FinFET SRAM highlights the need for optimization techniques to enhance its robustness and reliability.

As semiconductor technology continues to scale, FinFET-based memory architectures will play a crucial role in advancing energy-efficient computing systems. Future research can explore further optimizations in SRAM design, including novel circuit techniques and hybrid transistor architectures, to maximize performance. Overall, FinFET technology represents a significant advancement in SRAM design, paving the way for more efficient, compact, and high-performance memory solutions in emerging applications such as artificial intelligence, edge computing, and Internet-of-Things (IoT) devices.

Table 1 : Comparison between CMOS and FinFET

Performance parameters	CMOS	FinFET	% change in FinFET compare to CMOS
Average Power in write operation	124µW	8.76µW	92.92% reduction
Average Power in read operation	886.17nW	19.66nW	97.5% reduction

REFERENCES

1. “FinFET Technology based Low Power SRAM Cell Design for Embedded Memory" JV Suman, M Hema, AS Priya… - International …, 2024 - Computer systems rely heavily on cache memory because it offers a quicker and more effective means of accessing frequently used data. It serves as a buffer between the CPU(central processing unit) and main memory (RAM). Electronic devices' energy use during standby or idle mode is referred to as standby leakage, standby power consumption, or vampire power.
2. “Implementation and Analysis of 7T SRAM" - This paper analyzes the design of a 7T SRAM cell, highlighting performance improvements in terms of read speed and power leakage. Published by IEEE, 2023 (MDPI).
3. Design and implementation of 32nm FINFET based 4×4 SRAM cell array using 1-bit 6T SRAM. A. Lourts Deepak :VLSI system design, M. S. Ramaiah School of Advanced Studies, Bangalore, India Likhitha Dhulipalla:VLSI system design, M. S. Ramaiah School of Advanced Studies, Bangalore, India
4. FinFET SRAM design challenges David Burnett GLOBALFOUNDRIES, Global Memory Solutions, Austin, Santa Clara, CA, TX Sanjay PariharGLOBALFOUNDRIES, Global Memory Solutions, Austin, Santa Clara, CA,
5. Design and analysis of low power SRAM cells Akshay Bhaskar School of Electronics Engineering, VIT University, Vellore, India
6. A Review on SRAM Memory Design Using FinFET Technology T. Venkata Lakshmi, M. Kamaraju

7. J. Wuu, D. Weiss, C.Morganti, and M. Dreesen. The Asynchronous 24MB On-chip Level-3 Cache for a Dual-Core Itanium-Family Processor. ISSCC, 2005, 488–89.
8. E. Seevinck, F. J. List and J. Lohstoh. Static-Noise Margin Analysis of MOS SRAM Cells. JSSC, 1987, 366–77.
9. X. Huang et al. Sub-50nm P-Channel FinFET, IEDM Tech. Dig., 1999, 67–70.
10. A. J. Bhavnagarwala, X. Tang and J. Meindl. The Impact of Intrinsic Device Fluctuations on CMOS SRAM Cell Stability. JSSC, 2001, 658–665.
11. Reliability and energy efficiency of the tunneling transistor based 6T SRAM cell in sub-10nm domain IEEE Transactions on Circuits and Systems II (TCAS II)(2018)
12. Brain Swahn and Soha Hassoun (July 2006), Gate Sizing: FinFETs vs 32nm Bulk MOSFETs, In proceedings of DAC, Vol 2. pp. 218-224, California, USA.
13. Sharma VK, Pattanaik M. VLSI scaling methods and low power CMOS buffer circuit. *Journal of Semiconductors*. 2013; 34(9):095001.
14. Alioto M. Ultra-low power VLSI circuit design demystified and explained: a tutorial. *IEEE Transactions on Circuits and Systems I: Regular Papers*. 2012; 59(1): 3-29.
15. Roy K, Mukhopadhyay S, Mahmoodi-Meimand H. Leakage current mechanisms and leakage reduction techniques in deep-submicrometer CMOS circuits. *Proc IEEE*. 2003; 91(2): 305-327.
16. B. Yu, L. Chang, S. Ahmed et al., “FinFET scaling to 10 nm gate length,” in Proceedings of the IEEE International Devices Meeting (IEDM '02), pp. 251–254, San Francisco, Calif, USA, December 2002
17. Ming-Long Fan; Yu-Sheng Wu; Hu, V.P.-H.; Chien-Yu Hsieh; Pin Su; Ching-Te Chuang, "Comparison of 4T and 6T FinFET SRAM Cells for Subthreshold Operation Considering Variability—A Model-Based Approach," IEEE Transactions on Electron Devices,Vol.58, no.3, pp. 609,616, Mar. 2011.
18. Z. Guo, Shriram B., Radu Z., T. King, B. Nikolic, “FinFET based Design for Robust Nanoscale SRAM”, Proceeding of the international symposium on Low Power Electronics and design, pp 2-7, 2005.
19. A. N. Bhoj and N. K. Jha, “Design of logic gates and flip-flops in high-performance FinFET technology”, IEEE Transactions on Very Large Scale Integration (VLSI) Systems, vol. 21, no. 11, pp. 1975–1988, 2013.
20. Wenwei Yang, Zhiping Yu, Senior Member, IEEE, and Lilin Tian, “Scaling theory for FinFETs based on 3D effects investigation”, IEEE transactions on electron devices, vol. 54, no. 5, may 2007.f