International Journal for Multidisciplinary Research (IJFMR)
E-ISSN: 2582-2160 ● Website: www.ijfmr.com ● Email: editor@ijfmr.com

An Efficient and Improved Circuit of CMOS Comparator for Various Applications

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ABSTRACT
Now a days in digital interfacing, A/D converters, transmitting data, Squaring circuits, Phase discriminators voltage indicators and oscillating circuits. Comparators(CPs) are used to compare two voltages or currents. But when two voltages are similar then the resultant output is going to flicker between two possibilities which intends lead to the noise present in a comparator circuits are follow as unnecessary power consumption and produces a wrong result. To overcome this drawback we are designing a Two pair amplifier with an unbalanced differential stage where hysteresis concept is used to reduce the flickering of output and differential pair provides hysteresis bias current and form a current mirror of the transistor. The t_{pd} result shows two pair comparator which will give the better performance than comparator circuit with hysteresis. This project is used in A/D converters, Squaring circuits, Phase discriminators voltage indicators and oscillating circuits. The proposed comparator is fabricated in 180nm CMOS technology using cadence virtuso software and achieves a satisfactory performance.

Keyword: CP, A/D Convertors

1. INTRODUCTION:

A CP is circuit which has the two input signals and compares the two input signals if the difference voltage is +ve then the output voltage is positive saturation value,if the difference voltage is -ve then the output voltage is negative saturation value . While using small supply voltage it is difficult to compare high speed applications . In detail this high performance transistors with improved W/L values are required to reduce the power supply. Transistor thickness and extent are modify for low power consumption and high performance. The Hysteresis in the CP circuit is given to a little part of the O/P voltage to the +ve I/P. Hysteresis relate to the comparator circuit to reduce the circuit reactivity to noise and produce the output if the input in the state will be change slowly.A model for the comparator is designed and output isproduced and comparison results are obtained for theproposed model and the existing model. To design theexisting model we use Virtuoso tool.

2. EXISTING SYSTEM:

The two-stage CMOS amplifier is a first comparator with output inverter has threestages.Differential amplifier is the first stage, common-source amplifier is the second stage,and inverting buffer is the third stage. The I/P bias current is designated for 1micro ampere. The biascurrent of the proposed current mirror of two gain stages is 3µA. The two analog inputvoltages are connected to thedifferential pair. The voltage in this circuit is "Vim". In circuitdesign the speed is most important than the gain, the length of the transistor to be 0.18µm.NMOS transistors will give better results than PMOS transistors because they have better µ. NMOS differentialpair can be used.

The DP pair of NMOS transistor1and NMOS transistor2 will be improved due tothe gain ofthe first stage of the amplifier. A CS amplifier is used for the overallgainimprovement. The Aim is to reduce the capacitance of transistor PMOS2causes t_{pd} in the 1ststage and the area of CS transistor PMOS transistor2 will be increases. The 3rdstage will be high input impedance hence the ovrallgain and slewrate of the circuit increases. Fig.1 shows the circuit diagram.

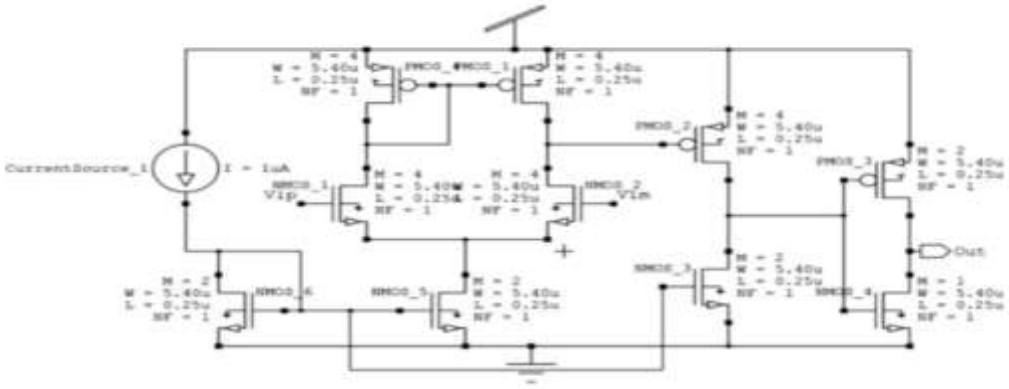


Fig. 1.First comparator: Output inverter of two stage CMOS amplifier

The first CP circuit shown in Fig.1 and have some problem and the comparison between the two analog inputs will be zero. In the comparator circuit output also caused by noise. The noise present in a comparator circuit are follow as unnecessary power consumption and produces a wrong result. In fig.2 The input noise signal cause the output.

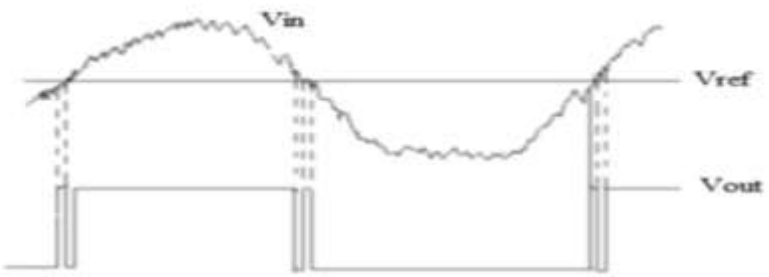


Fig 2: Comparator response to noise signal without hysteresis

3. PROPOSED SYSTEM:

Hysteresis concept is used to eliminate noise in the 1st CP circuit. Hysteresis is defined as difference between the UTP or (VTH) and LTP or VTL. It reduces circuit sensitivity and also number of transitions at the O/P. By using hysteresis the O/P of the CP is shown in below fig.3

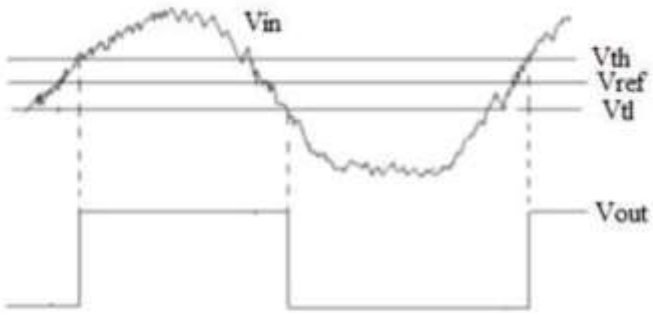


Fig 3: Comparator response to noise signal after adding hysteresis

To eliminate the noise in the circuit of the 1st CP circuit by using hysteresis. An unbalanced DP is added to the 1st comparator circuit by using programmable hysteresis. The simplified comparator circuit is shown in fig. 4

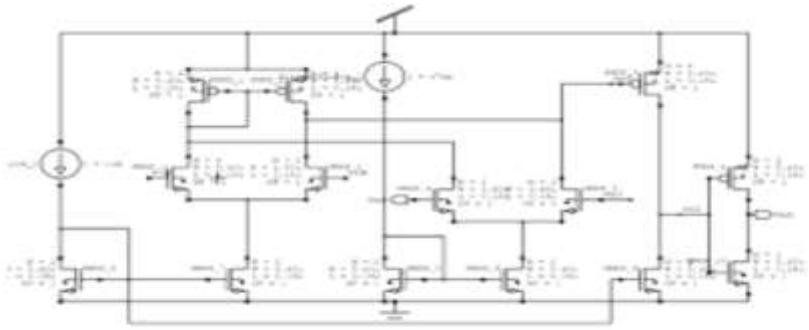
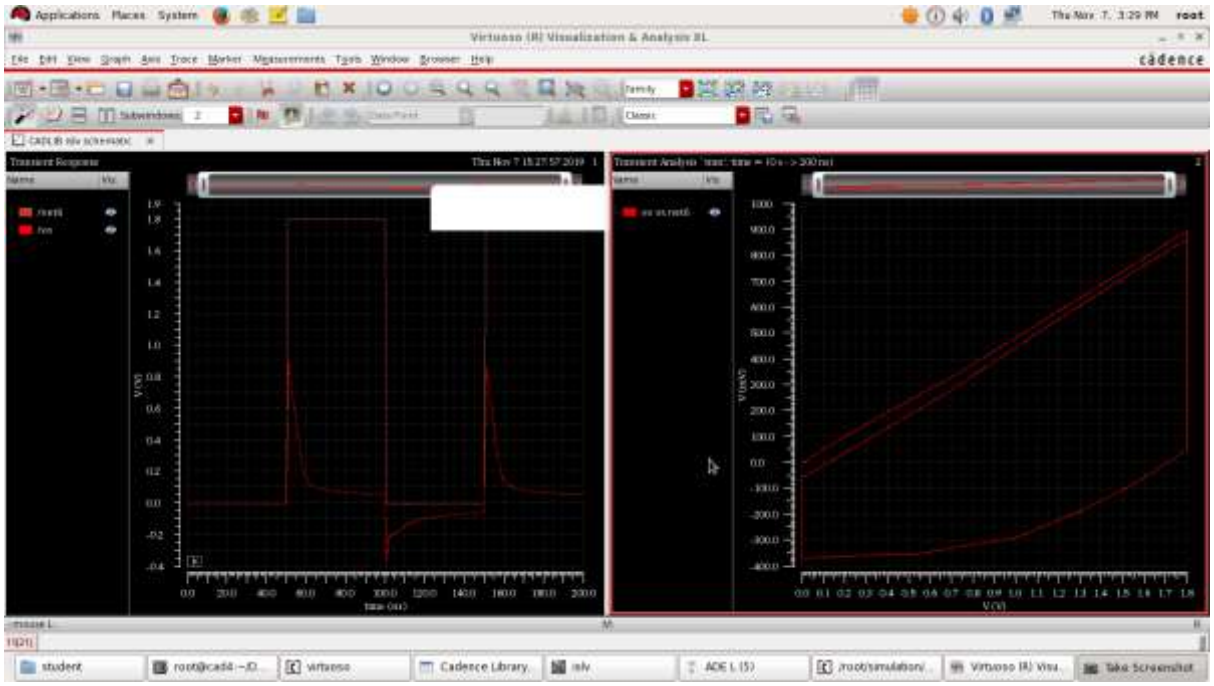


Fig 4: Second comparator: Two-Stage Amplifiers with an Unbalanced Differential Pair

Now a days everything is digitized but the signals are analog in nature. So we do need to change the analog signals into digital signals that's required ADC .The less t_{pd}high performance A/Ds,op-amps became a dominant role in high performance applications which can be implemented with minimum power and minimum power consumption devices which can be implemented with small size and process variation techniques. If we concentrate on small size the delay may be increases and there by performance decreases. Therefore, we design a CP circuit such that which meets and satisfies the all performance criterion, the various design issues related to speed, gain, power dissipation, offset and resolution are of paramount importance.

4. RESULT:



5. ADVANTAGES:

- Using low power supply we can run high speed applications.
- Noise is completely removed.

6. DISADVANTAGES:

- Circuits are difficult to implement.
- Some circuits are not practicable.

7. APPLICATIONS:

- Used in data transmission applications.
- Used in analog to digital converters.

8. CONCLUSION:

The CP circuit is implemented and simulated which is applicable for high speed A/Ds and various interfacing circuits.we designed 2nd comparator circuit which eliminates the noise. The effective way to implement the CP circuit is with180nmCMOSprocess The results obtained in this paper satisfy the expected functions of CP. It also compared the existing and proposed CP circuits with improved results.

REFERENCES:

1. Samaneh Babayan-Mashhadi and RejaLotfi “Analysis and Design of a Low-Voltage LowPower Double-Tail Comparator” IEEE Journal on VLSI system Vol. 22, feb. 2014.
2. V. B. Kulkarni, “Low-Power CMOS Comparators with Programmable Hysteresis,” Master Technical Report, ECE NMSU, 2005.
3. J. Wu, “A 100-MHz Pipelined CMOS Comparator,” IEEE Journal of Solid State Circuits, Vol. 23, No. 6, 1988, pp. 1379-1385. doi:10.1109/4.90034

4. P. E. Allen and D. R. Holberg, "CMOS Analog Circuit Design," 2nd Edition, Oxford University, Oxford, 2007.
5. B. Razavi, "Deign of Analog CMOS Integrated Circuits," Tata McGraw-Hill, Delhi, 2002.