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Techniques for Low-Power VLSI Systems: An Updated Overview

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Abstract
There is a rising demand for energy-efficient electronic devices in the context of portable, high-performance, and strongly embedded systems that warrant a serious concern and emphasis on low power Very Large-Scale Integration design. With the scaling of semiconductor technology at an aggressive pace of advancement, raised integration density and higher operating speeds introduce serious difficulties and challenges in effective power consumption management. This review paper examines the basic concepts of low power VLSI design and discusses the causes of dynamic and static power dissipation. It provides a systematic examination of numerous methods of power optimization developed at different levels of abstraction, starting from process technologies to digital circuits and architectural and systems levels. It is an attempt to present an overall detailed insight and perspective of present methodologies and means available to design VLSI circuits able to deliver superior performance at substantially lower energy dissipation levels.

Keywords: CMOS Technology Advancements, Architectural Level, Power Gating, Pipelining and Parallel Processing, Multi-Threshold CMOS.

1. Introduction:

One major historic force behind the development of VLSI technology is the scaling of performance and integration density. But because of the wide usage of cellular communication systems and computing systems everywhere, power dissipation in digital systems is turning out to be the most paramount limiting factor [1]. With the aggressive scaling of feature sizes down to nanoscales because of advancements in lithography technology, the transistor counts and operating speeds have exponentially increased and consequently power dissipation is rising exponentially too [2]. Consequently, low power design is proving to be absolutely necessary owing to the ever-growing needs of increased battery time of cellular phones and lower packaging and cooling expenses of computing systems [3]-[4].

The design of low power VLSI circuits is related to meeting the complicated trade-off between computing speed, silicon space, and energy consumption. The main difficulty is finding a good compromise between computational speed and power consumption [5]. The main sources of CMOS circuit power consumption are the dynamic components due to switching activities, and the static or leakage component, which becomes important at a deep submicron technology [4].

1.1 Literature Review:

Many studies have been conducted related to different aspects of VLSI design at low power. Early

studies by Meindl carried out in 1995 emphasized the impending need for low power micro-electronics, with predictions related to future challenges and opportunities related to this emerging technology [1], [6]. As the need arose with the advent of mobile technology, system-level power optimization tools and techniques came forward as shown by Benini and De Micheli in 2003 related to designing efficient hardware and software at a lower level [7].

More recently, the study conducted by Chandrakasan et al. offered some viewpoints and perspectives on tools and considerations for the design of low-voltage digital systems, a fundamental challenge of power reduction [8]. The study conducted by Alioto in 2012 offered a complete tutorial on the subject of ultra-low power VLSI circuit design, unifying complex viewpoints [9]. Recent summaries of the subject by Madhura and Raut et al. offered a collection of various models of low power VLSI designs [4],[5]. The viewpoints of Shan and Raghavendra, as well as Chandrashekar, extend the study of the subject into more contemporary perspectives of the current state of the subject, as well as the future developments of voltage scaling [2],[4],[10].

The future roadmap offered by Ramesh et al. shows the future of the subject pushing the emerging boundaries of reduced power consumption, investigating new transistors and devices [11][12].

2. Low Power Design Techniques:

Effective power reduction in VLSI systems requires a multi-level approach, encompassing design considerations from process technology to system-level architectures. Considering multiple power optimization strategies during VLSI design is important [2], [4],[13],[7].

Table 1: Multi-Level Power Optimization Strategy.

Level of Abstraction	Key Optimization Techniques	Description
Process Technology	Voltage scaling, advanced transistor structures, multi-threshold devices, negative- capacitance FETs, CMOS scaling innovations.	Improves fundamental device properties to reduce leakage and dynamic power through innovations in fabrication and transistor design.
Circuit & Logic Design	Switched-capacitance reduction, power modeling, ultra-low-power principles, clock gating, bus-invert coding.	Reduces switching activity and optimizes circuit structure using sizing, logic restructuring, and efficient encoding.
Architectural Level	Dynamic power management, energy-efficient architectures, approximate computing.	Optimizes system architecture to match workload needs, enabling major energy savings.
System Level & Software	DVFS, power gating, multi-threshold CMOS, software energy analysis.	Manages power at the whole-system level, leveraging hardware–software coordination to reduce energy consumption dynamically.

Table 1 illustrates that power optimization is necessarily hierarchical, and holistic methods need to be formulated across all levels of the design process in order to address overall power consumption efficiency. Every level of abstraction offers unique opportunities for saving power, and optimal low-

power VLSI design techniques can be achieved only by considering their interrelations. [2].

2.1Process Technology Level:

Optimizations on the process level aim at the basic physical properties of the devices themselves:

Aggressive Voltage Scaling: Scaling back the voltage () is proven to be one of the most effective methods to reduce power dissipation. Along with aggressive voltage scaling, optimization at different levels of technology and architectures is necessary in achieving ultra-low power design goals [8].

Advanced Transistor Architecture: The techniques of FinFETs, Gate-All-Around FETs, and Silicon-On-Insulator increase the energy efficiency performance by providing control over the channel of a transistor as well as lowering the leakage currents [8],[10]. The results prove that 'FinFETs' provide an optimal replacement for the normal MOS system at a nanoscale because they conserve less energy, eliminate the problem of 'short channel effects,' as well as minimize the 'leakage current' [14],[15]. GAA-FETs can be utilized for device scaling at a node below 3nm [16-17].

Figure 1 illustrates the transition from a Planar MOSFET to a FinFET to a Gate-All-Around (GAA) FET structure [19,20].

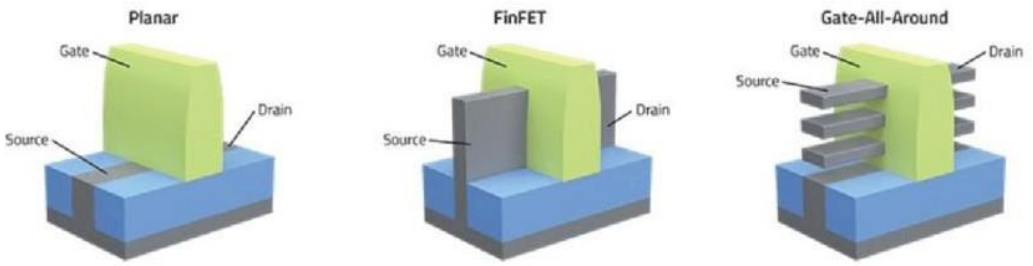

Figure 1: Comparative MOSFET → FinFET → GAAFET Diagram

Figure 1 shows the progression of transistor technology from Planar MOSFETs to FinFETs and, finally, to GAAFETs. Planar MOSFETs have a planar gate on top of a thin silicon channel with the source and drain on either side of it but are prone to short-channel effects below a node size of 45 nm. FinFETs enhance these by employing a three- dimensional vertical channel with a fin shape and a gate that goes around three sides of the fin but are still prone to leakage. This is further overcome by the GAAFET (Gate-All-Around FET), where the gate goes all the way around the channel, whether it is a nanosheet or a nanowire, resulting in excellent gate control below 5 nm but at the cost of increased complexity and complexity and increased cost of manufacturing.

Multiple-Threshold Devices: Using transistors with varying threshold voltages () enables one to optimize performance on critical paths (low V_T) and minimize static leakage currents on non-critical paths (high
V_T) [8].

Negative Capacitance: Currently, new research focuses on NC-FinFET devices, which have shown subthreshold swing values below the Boltzmann limit, allowing lower voltage operation and hence lower power dissipation. The devices are also better in suppressing the short channel effect Song, 2025.

CMOS Technology Advancements: Further research and development in CMOS technology, such as the pursuit of sub-10-nanometer gate technology, are very essential in the future design of low-power integrated circuits [12].

Figure 2 illustrates the progression of transistor technology: the basic planar MOSFET, 3D FinFET with a gate wrapped around, and the most advanced GAAFET with a gate completely wrapped around the

channel [21]. Such advancements significantly improved the control provided by the gate over the channel.

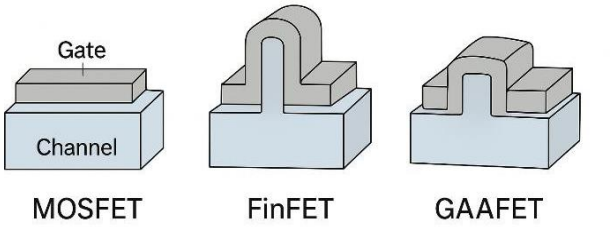

Figure 2: Evolution of MOS Transistor Architectures

The semiconductor industry has been constantly working to preserve the features and functionality of its devices as the device sizes have scaled down to smaller and smaller dimensions. The planar or classic MOS FETs comprise the more traditional form of the device, which has the gate layered on top of the silicon body and the silicon body surrounded on either side by the source and the drain regions. Though the planar FETs have worked well for devices of larger technology nodes, for smaller technology nodes, the devices have had poor electrostatics and higher leakage. The need for devices to preserve their functionality and have reduced power leakage and consumption has resulted in the innovation of the FET device, also known as the Fin-shaped Field Effect Transistor. It has a three-dimensional vertical structure with the shape of a fin. The gate covers the multiple-sided surfaces of the vertical fin structure. The improvements over the Fin-shaped Field Effect Transistor come with the introduction of the GAAFETs, which have the gate covering the device completely in the form of horizontal nanosheets and vertical nanowire FETs. The GAAFETs have the best possible gate control and will allow the devices to scale to smaller than 5nm sizes and effectively eliminate the device's Short Channel Effects.

2.2Circuit and Logic Design Level:

At the circuit level, techniques focus on minimizing switching activity and optimizing circuit configurations:

Reducing Switched Capacitance: One of the major techniques is to reduce the amount of capacitance that is switched. This is accomplished by using methods such as data-dependent shutdown and glitch removal [8].

Power Modeling and Optimization: The study of power modeling, estimation, and synthesis methods will enable the accounting for and optimization of power dissipation in the early stages of the design process [1].

Ultra-Low Power Design Principles: The need to understand specific design challenges and solutions related to ultra-low power designs, from circuit to micro-architecture, is critical to perform optimization [9].

Clock Gating: The clock signal to the inactive registers or functional units is disabled through this method to reduce switching activities, thus reducing dynamic power consumption [4].

A latch + AND gate clock-gating cell showing how the clock is gated before reaching registers in Figure 3 [22].

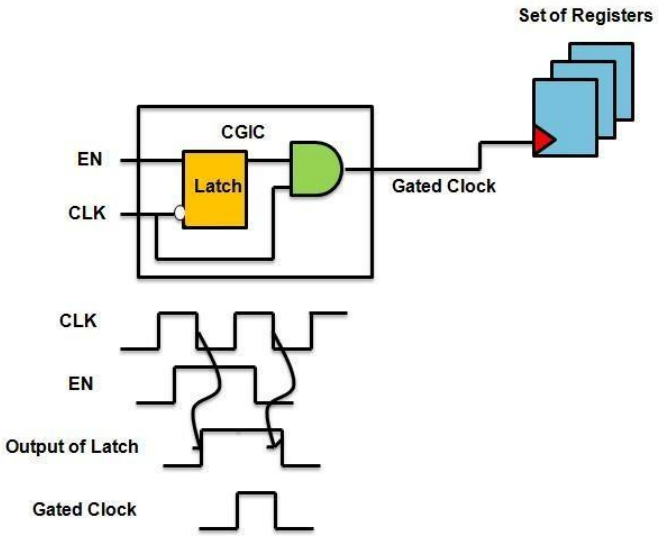

Figure 3: Clock Gating Integrated Cell

Clock gating can be considered a commonly applied method towards the reduction of dynamic power consumption in the context of synchronous digital circuits. The main intention behind the implementation of clock gating in such circuits revolves around the aspect that the clocks in these systems switch at the onset of every clock cycle. Further, the clocks in these systems control the flip-flops in the circuits. As a result, a substantial amount of dynamic power consumption in these systems occurs due to the unnecessary transition of the flip-flops in the modules being idle. The insertion of a gating logic in these systems, preferably in the form of an AND gate or an integrated gate cell (which consists of a latch and an AND gate), aims to make the clock input to a block dependent on an enable or a control signal. If the enable signal in the block is not active (implying a lack of new data or operation in the block), the gated clocks in such blocks refrain from toggling the flip-flops in the block. As a result, the dynamic power consumption in these blocks remains reduced.

Bus-Invert Coding: This method aims to reduce the switching activity on data buses by inverting the data when it leads to fewer transitions, thus lowering dynamic power dissipation [4].

2.3 Architectural

Architects' design decisions affect the system's power consumption as follows:

Dynamic Power Management: The techniques of DPM make it possible for systems to dynamically adjust to changes in workload. The result is energy savings achieved through changes in modes of operation [7].

Energy Efficient Architectures: New generations of architectures like Near-Threshold Computing, as well as asynchronous circuits, are being researched to reduce the power consumption by a substantial margin [13]. The main aim here is to run circuits at a supply voltage close to the threshold voltage of the transistor [18].

Approximate computing: This method makes use of the inherent error resilience within certain applications to conserve energy, at the same time trading off the computation accuracy slightly [13].

Pipelining and Parallel Processing: These methods can be applied to reduce the supply voltage and frequency to decrease the dynamic power consumption [4],[23].

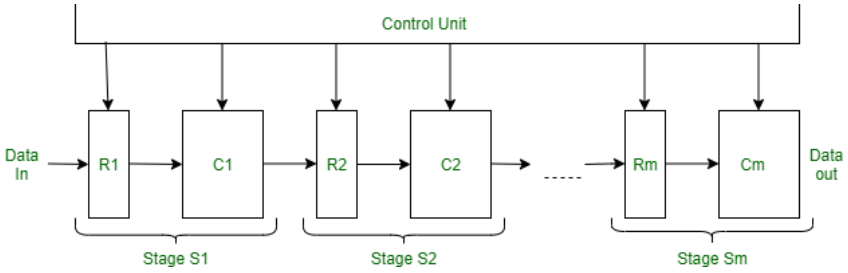

Figure 4: Structure of a Pipeline Processor

In Figure 4 above, pipelining is shown, where several tasks are performed simultaneously in stages, aiming at enhancing the instruction throughput, and parallel processing whereby several tasks or instructions are performed at the same time using several processing units that enhance system performance. Pipelining and parallel processing are basic concepts in computer architecture designs that aim at enhancing performance. Pipelining is where several tasks are performed in stages such as fetching, decoding, execution, and write back stages; hence several tasks are performed at the same time, like in an assembly line. A pipeline is full where several tasks are performed in one clock cycle, hence enhancing instruction throughput unlike in non-pipelined systems.

On the other hand, parallel processing involves the allocation of tasks to multiple processing units, either in a single multicore processor or in multiple processors, to enable multiple instructions or data streams to be processed at the same time. Such parallel processing may be done in independent processors or processor cores, unlike pipelining, in which multiple phases of the processing of a single stream of instructions are done contemporaneously.

Pipelining and parallel processing combine to propel today's computers closer to maximum throughput and efficiency. The efficiency is gained by overlapping work both at the level of instructions (pipelining) and across multiple execution facilities (parallel processing).

2.4System Level and Software Considerations

System-level and software aware designs play a vital role in optimizing the power consumption of the system as a whole:

System-Level Design Methods: Design methodologies for energy-efficient system-level design take into account hardware platforms and software components, examining approaches that decrease system energy usage in computation, communication, and storage components [7].

Dynamic Voltage and Frequency Scaling: DVFS is a popular method that varies the voltage and clock frequencies of a chip in functional units dynamically according to the applications' requirement of minimizing the power dissipation [13].

Power Gating: This requires the selective turning off of power to inactive circuit modules, thus reducing both dynamic and static power consumption of the inactive sections to near zeros [13],[25].

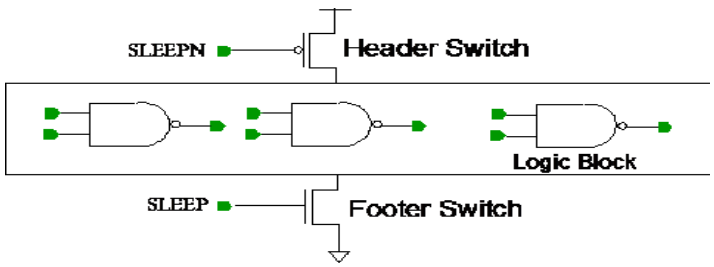

Figure 5: Power Gating Using Sleep Transistors

Power gating is a low power design technique at the circuit level, where sleep transistors (High threshold NMOS or PMOS transistors) are used between the power and ground and the logic block to turn off the power during idle periods, thus reducing the power during the standby mode, as shown in Figure 5.
Power gating is a common method in the leakage current reduction technique in VLSI design. This technique isolates unused blocks in the integrated circuits from the power supply in the idle/standby mode through sleep transistors acting as switches. These sleep transistors, either the header (PMOS) transistors or the footer (NMOS) transistors, are switched by a sleep signal. The transistors are turned off to make the path to the power/ground voltage "virtual" to isolate the logic block from the voltage and thus decrease the leakage current. The switch will be on in the active mode to make the block operate normally, whereas in the standby mode, turning off the switch's power consumption results in a substantial decrease in power consumption because the leakage current contributes greatly to the static power consumption in submicron CMOS processes [24].

2.5Power Design Technique

Multi-Threshold CMOS: On the system level, MTCMOS is harnessed to control the leakage power where high threshold voltage transistors are employed to turn off the power to the idle blocks [13].
Software Energy Cost Analysis: Energy cost analysis of software and the design of energy-consuming software are essential to the field of power management at the system level [7]. This involves low power compiler design and compiler instruction scheduling [4].

3.Conclusion

The development of low-power VLSI design techniques is now a basic need in the current era of electronics. This is due to the need for high-performance computing systems on one hand and the need for low-power portable systems on the other. As evidenced by this review, designing systems that can consume less power is a process that needs to incorporate a range of levels on the design abstraction hierarchy.An important step on this evolution path is the transition in the architectures of the transistors. With the aim of continuing to keep the electrostatic control and solve the issues of the short channels in the latest nodes, the technology transition from the classical planar MOSFET to 3-D architectures as FinFETs was successfully completed. The Gate-All-Around FETs represent the new wave, which is essential to achieve the scaling below the 5nm node.At the circuit level and architecture level, methods like clock gating, power gating with sleep transistors, and Dynamic Voltage Frequency Scaling (DVFS) have emerged as essential components for efficient management of dynamic as well as static power. In addition, developments in Multi-Threshold CMOS (MTCMOS) and Negative Capacitance (NC-FinFET) provide new promising directions for lowering the operating supply voltage without sacrificing system performance.
Ahead, the design environment faces many challenges, especially the increasing importance of static leakage power as device dimensions enter the nanometer regime. Although innovative technologies such as GAAFETs provide answers to these challenges, many manufacturing-related issues also arise. Indeed, if the physical limitations imposed by the present generation of Si technologies are to be overcome, it is necessary that attention shift towards more innovative technologies such as 3D IC integration, neuromorphic processors, and quantum computing systems. The eventual success of next-generation VLSI systems will depend on the seamless integration of all these seemingly disparate technologies that will effectively harmonize the need for computing power with the need for an earth-friendly environment.

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