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Linearity Enhanced Ultra-Wideband CMOS Low Noise Amplifier Using Active Feedforward and Weak Inversion Post Distortion Transistor

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Abstract
This paper presents a wideband Common-Gate Common-Source (CG-CS) Low Noise Amplifier (LNA) with enhanced linearity, designed and simulated in 45 nm GPDK045 CMOS technology using Cadence Virtuoso. The circuit extends an active feedforward noise-cancellation architecture by incorporating a post-distortion transistor M_{pd} permanently biased in the subthreshold (weak inversion) region. An active feedforward stage, composed of transistor M_{3n} and resistor R_3 in the main path, simultaneously achieves G_m-boosting, DC current reduction, and noise cancellation. The noise cancellation (NC) condition is $N = g_{m2}R_s$, whenever which both the common-gate device M_{1n} and the G_m-boost stage M_{3n} have their noise theoretically nulled at the output. Linearity is enhanced by the addition of transistor M_{pd}, with its gate connected to node Q (drain of M_{1n}) and its drain tied directly to output node S. By keeping M_{pd} in the subthreshold region via bias voltage V_{pd}, M_{pd} exhibits a positive third-order transconductance derivative $g''_{m,pd} > 0$ opposite to the compressive $g''_m < 0$ of the strong-inversion main-path transistors M_{1n} and M_2. A rigorous third-order Taylor-series nonlinear analysis confirms that the IM_3 intermodulation distortion (IM3) currents from M_{1n} and M_{3n}, already suppressed via the same NC mechanism as their noise, are further attenuated by the compensating nonlinear current injected by M_{pd}. Because M_{pd} conducts only microampere-level current in weak inversion, the IIP_3 improvement comes at negligible extra power. Pre-layout and post-layout Cadence Virtuoso simulations in GPDK045 validate the design for ultra-wideband (UWB) and 5G multi-standard receiver front-ends.

Keywords: Low Noise Amplifier (LNA), Active Feedforward, Gm-Boosting, Noise Cancellation, Post-Distortion, Weak Inversion, IIP3, Wideband, CMOS, GPDK045, UWB, 5G

1. Introduction

Modern wireless systems, especially 5G and emerging beyond-5G platforms, require RF front-end receivers that can handle multiple frequency bands without wasting power [2]. In any receiver chain, the Low Noise Amplifier (LNA) is the first active stage to process the incoming signal, so its noise and linearity figures directly set the overall receiver sensitivity and dynamic range. Designers working on multi-standard platforms face the simultaneous challenge of achieving flat gain, broadband input

matching, a low noise figure (NF), and a high third-order input intercept point (IIP3) all within a single compact integrated circuit [3].

Conventional wideband LNA topologies such as Common-Gate (CG) and Common-Source (CS) with resistive shunt feedback often have difficulties in achieving a low noise figure (NF) while maintaining good input matching over a wide frequency range, or suffer from limited gain and large power consumption [4]. The CG topology provides inherent wideband input matching through its low input impedance of approximately $\frac{1}{g_m}$, but its noise figure is fundamentally bounded near 3 dB due to the coupling between the input matching constraint and channel thermal noise [5]. The G_m-boosting technique relaxes this constraint by raising the effective transconductance without increasing the bias current [6, 7]. However, any active G_m-boost amplifier unavoidably adds thermal noise referred directly to the input [8]. Noise-cancellation (NC) techniques offer a way to break through the 3 dB NF floor. The underlying idea is to create anti-phase copies of a transistor's noise at two separate circuit nodes and arrange for them to cancel at the output while the wanted signal adds constructively [5, 9, 10]. Bruccoleri et al. first demonstrated this in a CG-CS balun-LNA that simultaneously achieves noise cancellation and a differential output [9]. Since then, many improved variants have appeared, using current-bleeding, local feedback, and current-mirror topologies to push NF, gain-bandwidth product, and power efficiency further [11–15].

Liu et al. [1] introduced an active feedforward architecture that achieves simultaneous current and noise reduction in a CG-CS LNA without violating the NC principle. By employing M_{3n} and R_3 as a feedforward G_m-boost stage in the main path, the DC current of the CG transistor M_{1n} drops below 1 mA, which reduces g_{m4} and thereby lowers the dominant FM_4 noise contribution. Crucially, [1] showed that the noise from M_{3n} and R_3 obeys the identical NC condition as M_{1n}, so both are theoretically suppressed. The NC condition is $N = g_{m2}R_s$, matching the standard CG-CS current-mirror topology. Although [1] achieves excellent NF and power efficiency, its linearity is constrained by the nonlinear behaviour of M_2 in the auxiliary path and residual nonlinearities from M_{1n} and M_{3n} in the main path. Post-distortion (PD) linearization addresses this by placing a secondary transistor at the output to inject a compensating nonlinear current [16, 17]. When biased in the subthreshold region, the PD transistor exhibits an exponential I-V characteristic that produces $g''_{m,pd} > 0$ opposite to the compressive $g''_m < 0$ of strong-inversion devices enabling third-order intermodulation distortion (IM3) cancellation with negligible power penalty [18].

This paper proposes a linearity-enhanced version of the active feedforward NC-LNA, implemented in 45 nm GPDK045 CMOS using Cadence Virtuoso, achieved by adding a single post-distortion transistor M_{pd} in the subthreshold region. The main contributions give: (1) a modified circuit topology incorporating M_{pd}; (2) proof that input matching and NC conditions are unchanged; (3) a complete third-order Taylor-series distortion analysis yielding the IIP3 expression and optimal cancellation condition under $N = g_{m2}R_s$ applied; and (4) physical explanation of the IIP3 improvement mechanism via M_{pd}.

The remainder of the paper is organized as follows. Section 2 reviews the base active feedforward NC-LNA. Section 3 presents the proposed circuit, covering input matching, noise cancellation, and the complete third-order distortion analysis. Section 4 discusses design trade-offs and presents GPDK045 simulation results. Section 5 compares the design against previously published wideband LNAs. Section 6 draws conclusions.

2. Active Feedforward CG-CS NC-LNA

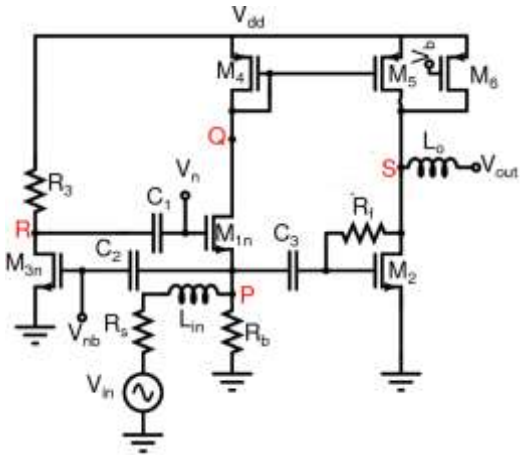

Fig. 1. Active feedforward CG-CS NC-LNA topology [1]

The circuit of Liu et al. [1] comprises a CG input transistor (M_{1n}) combined with an active feedforward Gm-boost stage (M_{3n} and R_3), a current-mirror (CM) network (M_4 and M_5) forming the main signal path, and a CS noise-cancellation stage (M_2) in the auxiliary path, as illustrated in Fig. 1. A current-bleeding (CBLD) transistor M_6 supplies the supplementary DC bias needed for a sufficiently large g_{m2} under the reduced g_{m4} and g_{m5} operating conditions. Two on-chip inductors L_{in} and L_o serve for broadband input matching and output bandwidth extension, respectively.

Key nodes in Fig.1 are: P is the RF input (source of M_{1n}), R is the G_m-boost output (gate of M_{1n}), Q is the drain of QM_{1n}, and S is the output node. The low-frequency input impedance is:

$$R_{in} = \frac{1}{g_{m1}\cdot(1 + g_{m3}\cdot R_3)} \quad \text{..... (1)}$$

The small-signal voltage gain from the RF input node P to output node S is:

$$A_v = -G_m \cdot R_{out} = -[N \cdot g_{m1} \cdot (1 + g_{m3} \cdot R_3) + g_{m2}] \cdot R_{out} \quad \text{..... (2)}$$

For complete suppression of the noise from M_{1n} at the output:

$$N = g_{m2} \cdot R_s \quad \text{..... (3)}$$

Combining equation (1) with equation (3) gives an equivalent form of the NC condition:

$$N \cdot g_{m1} \cdot (1 + g_{m3} \cdot R_3) = g_{m2} \quad \text{..... (4)}$$

A key result is that the noise produced by the G_m-boost stage (M_{3n} and R_3) follows the identical NC condition as M_{1n}. A noise voltage v_R at node R generates noise voltages v_P and v_Q at nodes P and Q with opposite polarities, which travel through the main and auxiliary paths and cancel at the output under equation (3).

3. Proposed Circuit with Post-Distortion Transistor

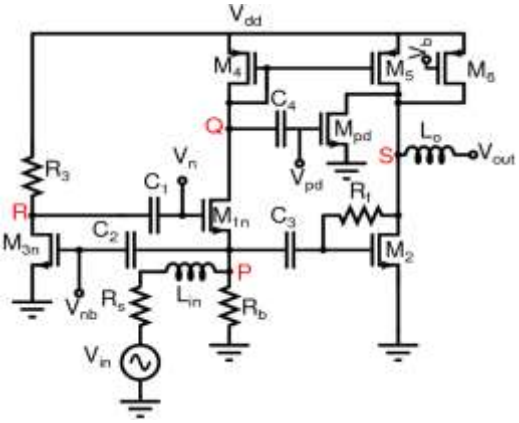

Fig. 2. Proposed linearity-improved CG-CS NC-LNA

The proposed design appends a single post-distortion transistor M_{pd}. The gate of M_{pd} connects to node Q (the drain of M_{1n}), while its drain connects directly to output node S. A DC bias voltage V_{pd} is fed to the gate via a high-resistance bias network, keeping M_{pd} permanently in the subthreshold region ($V_{pd} < V_{th} - \delta$), with a margin δ of 100–200 mV below threshold. The source of M_{pd} is grounded.

The circuit logic works as follows. Node Q carries the amplified, nonlinearity drain current of M_{1n} after G_m-boosting by M_{3n} and R_3. Connecting the gate of Q drives the gate of M_{pd}makes the IM3 current of M_{pd} correlated with the very distortion products arriving at node Q. Biasing M_{pd} in the subthreshold region yields $g''_{m,pd} > 0$, which injects a positive IM3 correction current into node S that partially or fully offsets the negative IM3 currents from M_{1N}, M_{3n} (mirrored via M_4/M_5), and M_2.

Since M_{pd} operates in weak inversion, its drain current stays in the microampere range. The total added power is $I_{D,pd} * VDD$, which is negligible. The voltage V_{pd} serves as the tuning parameter for cancellation depth. Since the subthreshold current depends exponentially on V_{pd} via $I_{D,pd} = I_0 \cdot \exp(\frac{V_{pd}}{nV_T})$, fine and sensitive control of the cancellation is achievable through small adjustments of V_{pd}.

3.1. Proposed circuit Implementation and Input Impedance Matching

The circuit is implemented in the 45 nm GPDK045 process library in Cadence Virtuoso. The slightly larger feature size introduces marginally higher threshold voltages but comparable RF performance; inductor values and transistor sizing are re-optimised accordingly. The addition of M_{pd} does not change the input impedance because M_{pd} connects at node Q (the drain of M_{1n}) and at S (output) neither is the RF input port P. The low-frequency input impedance therefore stays:

$$R_{in} = \frac{1}{g_{m1} \cdot (1 + g_{m3} \cdot R_3)} \quad \text{..... (5)}$$

Three parameters jointly set the input impedance: g_{m1}, g_{m3}, and R_3. To meet the 50 Ω matching target ($R_{in} = R_s = 50\ \Omega$), R_3 can be increased to permit smaller g_{m1} and g_{m3} for reduced current dissipation, enabling sub-1 mA operation of M_{1n}. For broadband input matching, an L-type network with on-chip inductor L_{in} holds S_{11} below −10 dB across the UWB band. The input capacitance at node P is dominated by the gate-source capacitances of M_{1n}, M_2, and M_{3n}, giving a dominant input pole:

$$\omega_P = \frac{1}{(C_{gs1} + C_{gs2} + C_{gs3})\cdot(R_s \parallel R_{in})} \quad \text{..... (6)}$$

Under the matched condition $R_{in} = R_s$ the following simplified relation holds:

$$g_{m1} \cdot (1 + g_{m3} \cdot R_3) = \frac{1}{R_s} \Rightarrow g_{m1,eff} = \frac{1}{R_s} \quad \text{..... (7)}$$

3.2. Noise Cancellation Analysis

3.2.1 Noise Cancellation of M_{1n}

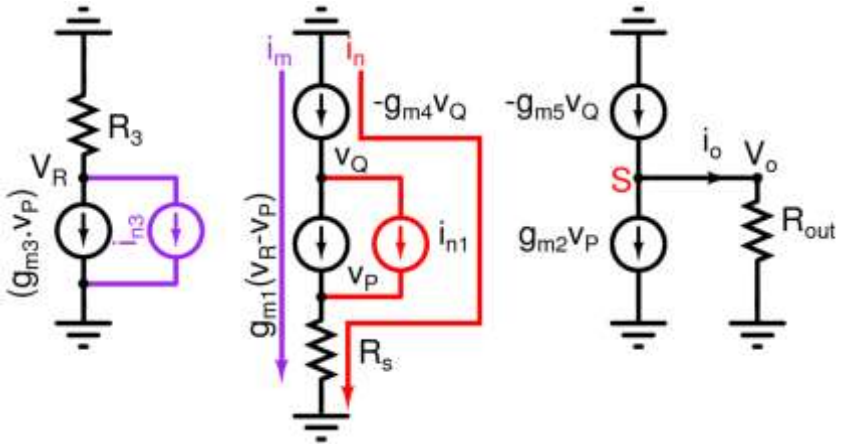

Fig. 3. Small-signal noise model for noise cancellation analysis

Using a KCL-based small-signal noise analysis (Fig. 3), the thermal channel noises of M_{1n} and M_{3n} are represented by current sources i_{n1} and i_{n3} respectively. For the noise current in the main path due to i_{n1}, KCL at nodes R, P, and Q are:

$$v_R = -g_{m3} \cdot v_P \cdot R_3 \quad \text{..... (8)}$$

$$v_P = i_n \cdot R_s \quad \text{..... (9)}$$

$$v_Q = -\frac{i_n}{g_{m4}} \quad \text{..... (10)}$$

$$i_n = i_{n1} + g_{m1} \cdot (v_R - v_P) \quad \text{..... (11)}$$

Solving this system of equations gives:

$$i_n = \frac{i_{n1}}{1 + g_{m1}\cdot R_s \cdot (1 + g_{m3}\cdot R_3)} \quad \text{..... (12)}$$

Under the input matching condition (equation 7), this simplifies to $i_n = \frac{i_{n1}}{2}$, confirming that half the noise current of M_{1n} flows through the main path. For complete cancellation of M_{1n} at the output, the required condition is:

$g_{m5} \cdot v_Q + g_{m2} \cdot v_P = 0$..... (13)

Substituting $v_P = i_n \cdot R_s$ and $v_Q = -\frac{i_n}{g_{m4}}$ and simplifying recovers the NC condition:

$N = g_{m2} \cdot R_s$..... (14)

3.2.2 Noise Cancellation of M_{3n} and R_3

The noise from the G_m-boost stage M_{3n} and resistor R_3 obeys the identical NC procedure as M_{1n}. Treating M_{3n} as representative, a noise voltage v_R at node R generates two noise voltages v_P and v_Q at nodes P and Q with opposite polarities. Treating i_m as the current driven by v_R (Fig. 3), the KCL equations are:

$v_R = -(i_{n3} + g_{m3} \cdot v_P) \cdot R_3$..... (15)

$v_P = i_m \cdot R_s$..... (16)

$v_Q = -\frac{i_m}{g_{m4}}$..... (17)

$i_m = g_{m1} \cdot (v_R - v_P)$..... (18)

Solving similarly:

$i_m = \frac{-i_{n3} \cdot R_3 \cdot g_{m1}}{1 + g_{m1} \cdot R_s \cdot (1 + g_{m3} \cdot R_3)}$ ..... (19)

Under input matching this reduces to $\frac{-i_{n3} \cdot R_3 \cdot g_{m1}}{2}$. Applying equation (13) to find the NC condition for M_{3n} recovers equation (14). Consequently, the NC principle of the G_m-boost stage is identical to that of the main amplifier, and both M_{1n} and M_{3n} noise sources are suppressed at node S under $N = g_{m2} \cdot R_s$

3.2.3 Noise Contribution of M_{pd}

The drain current noise of M_{pd} in weak inversion has a power spectral density of $4KT\gamma g_{mpd}$. Given that $g_{mpd} = \frac{I_{D,pd}}{nV_T}$ and $I_{D,pd}$ is in the microampere range, g_{mpd} is much smaller than g_{m1}, g_{m2}, or g_{m4}. The output-referred noise contribution of M_{pd} is therefore negligible relative to the dominant contributions from M_2 andM_4 . Under the NC condition, the simplified noise factor of the proposed circuit is:

$F = 1 + \frac{\gamma}{N} + \gamma \cdot g_{m4} \cdot R_s + \frac{\gamma \cdot g_{m4} \cdot R_s}{N} + \frac{\gamma \cdot g_{m6} \cdot R_s}{N^2} + \frac{\gamma \cdot g_{m,pd} \cdot R_s}{N^2}$ ..... (20)

The last term represents the added noise of M_{pd}, which is suppressed by N^2 in the denominator and by the small $g_{m,pd}$ making its contribution negligible. The dominant noise sources remain M_2 and M_4.

3.3. Linearity Analysis and IIP_3 Derivation

3.3.1. Nonlinear MOSFET Model

MOSFET nonlinearity is represented as a current source controlled by V_{gs} connected between source and drain. Neglecting the output conductance nonlinearity g_{ds}, the drain current is expressed as a Taylor series in V_{gs}:

$$i_{ds} = g_m \cdot v_{gs} + \frac{g'_m}{2!} \cdot {v_{gs}}^2 + \frac{g''_m}{3!} \cdot {v_{gs}}^3 + \cdots = g_m \cdot v_{gs} + i_{NL} \quad \text{..... (21)}$$

Here the first- and second-order transconductance derivatives are:

$$g'_m = \frac{\partial^2 I_{ds}}{\partial {V_{gs}}^2}, \quad g''_m = \frac{\partial^3 I_{ds}}{\partial {V_{gs}}^3} \quad \text{..... (22)}$$

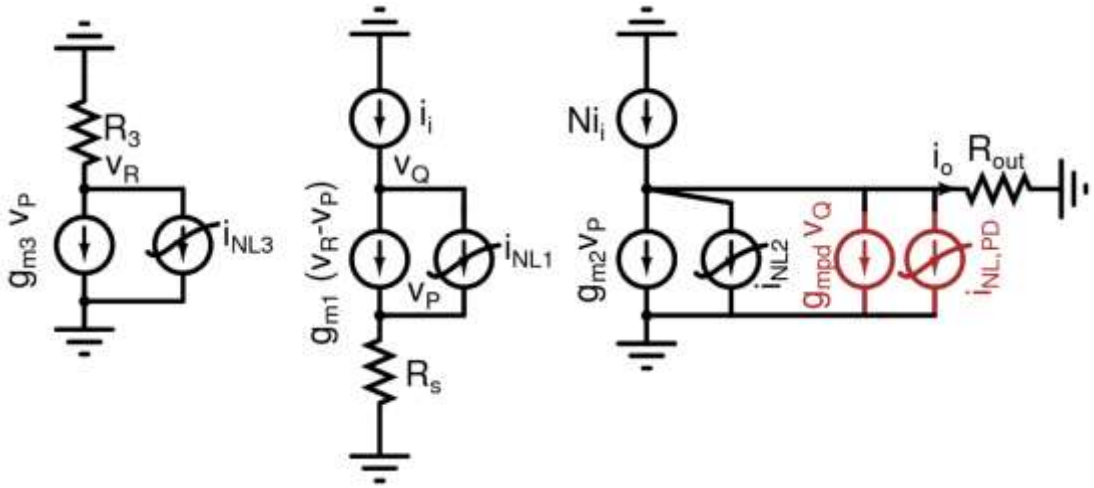

Fig. 4. Small-signal model of the proposed circuit for distortion analysis

Third-order nonlinear contributions from M_{1n}, M_2 and M_{3n} and M_{pd} are included up to third order (Fig. 4); current-mirror nonlinearity is neglected for simplicity. For transistors M_{1n}, M_2, M_{3n} biased in strong inversion (saturation), $g''_m < 0$ due to mobility degradation and velocity saturation effects, causing gain compression. For M_{pd} in the subthreshold region, the exponential I-V relationship yields $g''_{m,pd} > 0$, representing gain expansion, which provides the distortion cancellation mechanism.

3.3.2 KCL Equations at Nodes *R* and *P*

Taylor-series expansions for the output current i_{out} as a function of source voltage v_s are found by applying KCL at nodes v_R and v_P in Fig. 4:

$$i_1 = g_{m1} \cdot (v_R - v_P) + \frac{g'_{m1}}{2} \cdot (v_R - v_P)^2 + \frac{g''_{m1}}{6} \cdot (v_R - v_P)^3 \quad \text{..... (23)}$$

$$v_s = v_P - i_1 \cdot R_s \quad \text{..... (24)}$$

$$-\frac{v_R}{R_3} = g_{m3} \cdot v_P + \frac{g'_{m3}}{2} \cdot {v_P}^2 + \frac{g''_{m3}}{6} \cdot {v_P}^3 \quad \text{..... (25)}$$

where i_1 is the drain current of M_{1n}. g'_{mi} and g''_{mi} $(i = 1,2,3)$ are the first- and second-order derivatives of the transconductance of M_{1n}, M_2, and M_{3n} respectively. Solving the above system expresses v_s as a power series:

$$v_s = a_1 \cdot v_P + a_2 \cdot {v_P}^2 + a_3 \cdot {v_P}^3 \text{..... (26)}$$

where the power-series coefficients are:

$$a_1 = g_{m1} \cdot (g_{m3} \cdot R_3 + 1) \cdot R_s + 1 \text{..... (27)}$$

$$a_2 = \frac{R_s}{2} \cdot [g_{m1} \cdot {g'}_{m3} \cdot R_3 - {g'}_{m1} \cdot (g_{m3} \cdot R_3 + 1)^2] \text{ ..... (28)}$$

$$a_3 = [\frac{1}{6} \cdot g_{m1} \cdot {g''}_{m3} \cdot R_3 - \frac{1}{2} \cdot {g'}_{m1} \cdot {g'}_{m3} \cdot (g_{m3} \cdot R_3 + 1) + \frac{1}{6} \cdot {g''}_{m1} \cdot (g_{m3} \cdot R_3 + 1)^3] \cdot R_s \text{..... (29)}$$

3.3.3 Inverse Power Series for v_P in Terms of v_s

Inverting equation (26), v_P is expressed in terms of v_s :

$$v_P = b_1 \cdot v_s + b_2 \cdot {v_s}^2 + b_3 \cdot {v_s}^3 \text{ ..... (30)}$$

where the series inversion coefficients are:

$$b_1 = \frac{1}{a_1} \text{ ..... (31)}$$

$$b_2 = -\frac{a_2}{{a_1}^3} \text{..... (32)}$$

$$b_3 = \frac{2{a_2}^2}{{a_1}^5} - \frac{a_3}{{a_1}^4} \text{ ..... (33)}$$

Under the input matching condition (equation 7), $a_1 = 2$ and therefore $b_1 = \frac{1}{2}$. The higher-order coefficients b_2 and b_3 retain their symbolic forms depending on the circuit parameters, and are not substituted with numerical values in this analysis to preserve generality.

3.3.4 Drain Currents of M_{1n} and M_2

The drain current of M_{1n}, i_1, is written:

$$i_1 = \frac{(b_1 - 1) \cdot v_s + b_2 \cdot {v_s}^2 + b_3 \cdot {v_s}^3}{R_s} \text{..... (34)}$$

The drain current of M_2, i_2 is written as:

$$i_2 = g_{m2} \cdot v_P + {g'}_{m2} \cdot {v_P}^2 + {g''}_{m2} \cdot {v_P}^3 \text{..... (35)}$$

Substituting v_P from equation (30) and grouping by order:

$$i_2{}^{(1)} = g_{m2} \cdot b_1 \cdot v_s \text{..... (36)}$$

$$i_2{}^{(2)} = [g_{m2} \cdot b_2 + \frac{g'_{m2}}{2} \cdot b_1{}^2] \cdot v_s{}^2 \text{..... (37)}$$

$$i_2{}^{(3)} = [g_{m2} \cdot b_3 + g'_{m2} \cdot b_1 \cdot b_2 + \frac{g''_{m2}}{6} \cdot b_1{}^3] \cdot v_s{}^3 \text{..... (38)}$$

3.3.5 Voltage at Node Q and Current of M_{1n}

Node SQM_{1n} loaded by $\frac{1}{g_{m4}}$. Defining $\beta = \frac{1}{g_{m4}R_S}$

$$v_Q = -\frac{i_1}{g_{m4}} = -\beta \cdot (b_1 - 1) \cdot v_s - \beta \cdot b_2 \cdot v_s{}^2 - \beta \cdot b_3 \cdot v_s{}^3 \text{..... (39)}$$

Since $b_1 = \frac{1}{2}$, the coefficient $(b_1 - 1) = -\frac{1}{2}$ so:

$$v_Q = \frac{\beta}{2} \cdot v_s - \beta \cdot b_2 \cdot v_s{}^2 - \beta \cdot b_3 \cdot v_s{}^3 \text{..... (40)}$$

M_{pd} gate connects to node Q, therefore $V_{gs,pd} = V_Q$. In weak inversion, $g''_{m,pd} > 0$:

$$i_{pd} = g_{m,pd} \cdot v_Q + \frac{g'_{m,pd}}{2} \cdot v_Q{}^2 + \frac{g''_{m,pd}}{6} \cdot v_Q{}^3 \text{..... (41)}$$

Substituting equation (40) into (41) and collecting terms by order in vs gives:

$$i_{pd}{}^{(1)} = g_{m,pd} \cdot \frac{\beta}{2} \cdot v_s \text{..... (42)}$$

$$i_{pd}{}^{(2)} = [-g_{m,pd} \cdot \beta \cdot b_2 + \frac{g'_{m,pd}}{2} \cdot (\frac{\beta}{2})^2] \cdot v_s{}^2 \text{..... (43)}$$

$$i_{pd}{}^{(3)} = [-g_{m,pd} \cdot \beta \cdot b_3 - g'_{m,pd} \cdot \frac{\beta}{2} \cdot \beta \cdot b_2 + \frac{g''_{m,pd}}{6} \cdot (\frac{\beta}{2})^3] \cdot v_s{}^3 \text{..... (44)}$$

The simplified third-order component of M_{pd}:

$$i_{pd}{}^{(3)} = [-g_{m,pd} \cdot \beta \cdot b_3 - \frac{g'_{m,pd} \cdot \beta^2 \cdot b_2}{2} + \frac{g''_{m,pd} \cdot \beta^3}{48}] \cdot v_s{}^3 \text{..... (45)}$$

3.3.6 KCL at Output Node S

Applying KCL at node S in Fig. 4, and extending equation (22) to include M_{pd}:

$$i_{out} = N \cdot i_1 - i_2 - i_{pd} \text{..... (46)}$$

In Fig.1, without M_{pd}, the KCL reduces to $i_{out} = N \cdot i_1 - i_2$. Substituting equations (34)–(38) and (42)–(45) into equation (46), and collecting by order:

First-order component:

$$i_{out}^{(1)} = [\frac{N\cdot(b_1-1)}{R_s} - g_{m2}\cdot b_1 - g_{m,pd}\cdot\frac{\beta}{2}]\cdot v_s \text{..... (47)}$$

Second-order component:

$$i_{out}^{(2)} = [\frac{N\cdot b_2}{R_s} - g_{m2}\cdot b_2 - \frac{g'_{m2}}{2}\cdot b_1^{\,2} + g_{m,pd}\cdot\beta\cdot b_2 - \frac{g'_{m,pd}}{8}\cdot\beta^2]\cdot v_s^{\,2} \text{..... (48)}$$

Third-order component:

$$i_{out}^{(3)} = [\frac{N\cdot b_3}{R_s} - g_{m2}\cdot b_3 - g'_{m2}\cdot b_1\cdot b_2 - \frac{g''_{m2}}{6}\cdot b_1^{\,3} + g_{m,pd}\cdot\beta\cdot b_3 + \frac{g'_{m,pd}\cdot\beta^2\cdot b_2}{2} - \frac{g''_{m,pd}\cdot\beta^3}{48}]\cdot v_s^{\,3} \text{..... (49)}$$

3.3.7 Apply Noise Cancellation Condition $N = g_{m2}R_s$

Substituting the NC condition $N = g_{m2}R_s$, i.e., $g_{m2} = \frac{N}{R_s}$, together with $b_1 = \frac{1}{2}$, so $(b_1 - 1) = -\frac{1}{2}$ and $(1 - 2b_1) = 0$:

First-order simplification — the g_{m2} terms cancel, giving:

$$\frac{N\cdot(b_1-1)}{R_s} - g_{m2}\cdot b_1 = g_{m2}\cdot(b_1 - 1) - g_{m2}\cdot b_1 = -g_{m2} \text{..... (50)}$$

The first-order output current including M_{pd} becomes:

$$i_{out}^{(1)} = -[g_{m2} + g_{m,pd}\cdot\frac{\beta}{2}]\cdot v_s \text{..... (51)}$$

After applying the NC condition, the second-order term becomes:

$$i_{out}^{(2)} = -[\frac{g'_{m2}}{2}\cdot b_1^{\,2} - g_{m,pd}\cdot\beta\cdot b_2 + \frac{g'_{m,pd}}{8}\cdot\beta^2]\cdot v_s^{\,2} \text{ ..... (52)}$$

And the third-order term becomes:

$$i_{out}^{(3)} = -[g'_{m2}\cdot b_1\cdot b_2 + \frac{g''_{m2}}{6}\cdot b_1^{\,3} - g_{m,pd}\cdot\beta\cdot b_3 - \frac{g'_{m,pd}\cdot\beta^2\cdot b_2}{2} + \frac{g''_{m,pd}\cdot\beta^3}{48}]\cdot v_s^{\,3} \text{ ..... (53)}$$

3.3.8. Complete Simplified Output Current

After applying $N = g_{m2}R_s$ and $b_1 = \frac{1}{2}$, the complete output current is:

$$i_{out}^{(1)} = -\left[g_{m2} + g_{m,pd} \cdot \frac{\beta}{2}\right] \cdot v_s - -\left[\frac{g'_{m2}}{2} \cdot {b_1}^2 - g_{m,pd} \cdot \beta \cdot b_2 + \frac{g'_{m,pd}}{8} \cdot \beta^2\right] \cdot {v_s}^2 - [g'_{m2} \cdot b_1 \cdot b_2 + \frac{g''_{m2}}{6} \cdot {b_1}^3 - g_{m,pd} \cdot \beta \cdot b_3 - \frac{g'_{m,pd} \cdot \beta^2 \cdot b_2}{2} + \frac{g''_{m,pd} \cdot \beta^3}{48}] \cdot {v_s}^3 \quad \text{..... (54)}$$

Setting M_{pd} ($g_{m,pd} = 0$), equation (54)-(57) reduces to

$$i_{out}|_{\text{w/o } M_{pd}} = -g_{m2} \cdot v_s - \frac{g'_{m2}}{2} \cdot {b_1}^2 \cdot {v_s}^2 - [g'_{m2} \cdot b_1 \cdot b_2 + \frac{g''_{m2}}{6} \cdot {b_1}^3] \cdot {v_s}^3 \quad \text{..... (58)}$$

3.3.9. IIP_3 Expression

Defining the total first-order coefficient as G_{m1} and third-order coefficient as G_{m3}:

$$G_{m1} = g_{m2} + g_{m,pd} \cdot \frac{\beta}{2} \quad \text{..... (59)}$$

$$G_{m3} = g'_{m2} \cdot b_1 \cdot b_2 + \frac{g''_{m2}}{6} \cdot {b_1}^3 - g_{m,pd} \cdot \beta \cdot b_3 - \frac{g'_{m,pd} \cdot \beta^2 \cdot b_2}{2} + \frac{g''_{m,pd} \cdot \beta^3}{48} \quad \text{..... (60)}$$

The $IIP3$ of the proposed circuit is:

$$IIP3 = \sqrt{\frac{4}{3} \cdot \left|\frac{G_{m1}}{G_{m3}}\right|} \quad \text{..... (61)}$$

$$IIP3 = \sqrt{\frac{4}{3} \cdot \left|\frac{g_{m2} + g_{m,pd} \cdot \frac{\beta}{2}}{G_{m3}}\right|} \quad \text{..... (62)}$$

Setting M_{pd}, equation (62) reduces to equation

$$IIP3|_{\text{w/o } M_{pd}} = \sqrt{\frac{4}{3} \cdot \left|\frac{g_{m2}}{g'_{m2} \cdot b_1 \cdot b_2 + \frac{g''_{m2}}{6} \cdot {b_1}^3}\right|} \quad \text{..... (63)}$$

3.3.10. Distortion Cancellation Condition

Peak IIP3 is obtained when $G_{m3} \rightarrow 0$. Setting the numerator coefficient of equation (62) to zero gives the cancellation condition:

$$\frac{g''_{m,pd} \cdot \beta^3}{48} + \frac{g'_{m,pd} \cdot \beta^2 \cdot b_2}{2} + g_{m,pd} \cdot \beta \cdot b_3 = g'_{m2} \cdot b_1 \cdot b_2 + \frac{g''_{m2}}{6} \cdot {b_1}^3 \quad \text{..... (64)}$$

The left side is positive because $g''_{m,pd} > 0$ and $g'_{m,pd} > 0$ in weak inversion, while b_2,b_3 are small correction terms. The right side is negative because $g''_{m2} < 0$ and $g'_{m2} < 0$ in strong inversion. The dominant cancellation mechanism is via the $g''_{m,pd}$ term:

$$\frac{g''_{m,pd} \cdot \beta^3}{48} \approx g'_{m2} \cdot b_1 \cdot b_2 + \frac{g''_{m2}}{6} \cdot {b_1}^3 \quad \text{..... (65)}$$

Since M_{pd} operates in weak inversion:

$$g''_{m,pd} = \frac{I_{D,pd}}{(\mathrm{n}V_T)^3} = \frac{I_0 \cdot \exp(\frac{V_{pd}}{\mathrm{n}V_T})}{(\mathrm{n}V_T)^3} \text{..... (66)}$$

Substituting equation (66) into (65), the analytically optimal gate bias for peak IIP3 is:

$$V_{pd,opt} = \mathrm{n}V_T \cdot \ln\left(\frac{48 \cdot (\mathrm{n}V_T)^3 \cdot |g'_{m2} \cdot b_1 \cdot b_2 + \frac{g''_{m2}}{6} {b_1}^3|}{I_0 \cdot \beta^3}\right) \quad \text{..... (67)}$$

Equation (67) demonstrates that V_{pd} can be computed from known circuit parameters. The exponential dependence of $g''_{m,pd}$ on V_{pd} via equation (66) enables very fine, sensitive control of the cancellation depth.

3.3.11. Physical Interpretation of Distortion Cancellation

Table 1. Distortion Contributions at Output Node SSource	**Third-Order Expression**	**Sign**	**Via**	**Net Effect**
$M_{1n} + M_{3n}$	Cancelled via NC condition (same as noise)	0	Current Mirror + M_2	Cancelled
M_2 (direct path)	$g'_{m2} \cdot b_1 \cdot b_2 + \frac{g''_{m2}}{6} \cdot {b_1}^3$	-	Auxiliary path	Limits IIP3
M_{pd} (2nd-order mixing)	$\frac{g'_{m,pd} \cdot \beta^2 \cdot b_2}{2}$	+	Post-distortion path	Partial cancellation
M_{pd} (direct 3rd)	$\frac{g''_{m,pd} \cdot \beta^3}{48}$	+	Post-distortion path	Primary cancellation

G_{m3} total	$G_{m3M2} + G_{m3Mpd} \rightarrow 0$	$\rightarrow 0$	Node S	IIP3 $\rightarrow \infty$

In summary, the IM3 currents from M_{1n} and M_{3n} are suppressed by the same NC mechanism as their noise contributions. The dominant LNA distortion therefore originates from M_2. The proposed M_{pd} in weak inversion supplies a positive G_{m3Mpd} that offsets the negative G_{m3M2}, driving G_{m3},total toward zero and substantially improving IIP3.

4. Design Considerations and GPDK045 Simulation Results

4.1. Independent Optimisation of Noise and Linearity

A key advantage of the proposed topology is that the NC condition $N = g_{m2}R_s$ sets the transconductance of M_2, fixing the dominant distortion coefficient G_{m3M2} via g''_{m2} and g'_{m2}. The distortion cancellation condition (equation 64) is independently satisfied by adjusting V_{pd}, which controls $g''_{m,pd}$ exponentially via equation (66). This decoupling is a key design advantage: NF and IIP3 are optimised through separate parameters without conflicting constraints. NF is fully preserved because M_{pd} does not participate in the NC loop.

4.2 Weak Inversion Biasing of M_{pd}

For M_{pd} to remain in the subthreshold region throughout normal operation, V_{pd} must satisfy $V_{pd} < V_{th} - \delta$, where δ is approximately 100–200 mV. The subthreshold drain current follows $I_{D,pd} = I_0 \cdot \exp(\frac{V_{pd}}{nV_T})$, where n is the subthreshold slope factor (typically 1.2–1.5) and $V_T = \frac{KT}{q}$ is the thermal voltage (26 mV at 300 K). The transconductance derivatives in weak inversion are:$V_T = 26\ mv$

$$g_{m,pd} = \frac{I_{D,pd}}{nV_T},\quad g'_{m,pd} = \frac{I_{D,pd}}{(nV_T)^2},\quad g''_{m,pd} = \frac{I_{D,pd}}{(nV_T)^3} \quad \text{..... (68)}$$

With $I_{D,pd}$ ranging from 10 to 100 µA and $nV_T \approx 35$ mV, $g_{m,pd}$ spans 0.28–2.8 mS. The exponential sensitivity of $g''_{m,pd}$ to V_{pd} enables fine tuning of the cancellation depth, but also introduces sensitivity to temperature (because $V_T = \frac{KT}{q}$ varies with T) and process variation. A temperature-compensated bias generator is advisable for robust production implementation.

4.3. Bandwidth Impact of Adding M_{pd}

The addition of M_{pd} introduces a small parasitic drain capacitance $C_{D,pd}$ at output node S. This increments the total output capacitance C_{out}, slightly detuning the resonance established by L_o. Inductor L_o is tuned to resonate with the updated C_{out} to restore bandwidth-extension peaking at the target frequency. Since M_{pd} is sized small with $I_{D,pd}$ in the microampere range, its W/L ratio is compact and $C_{D,pd}$ is negligible relative to the capacitances of M_2, M_5, and M_6 at node S. Consequently, bandwidth is essentially unaffected by the addition of

4.4. Simulation Results

Pre-layout and post-layout simulations were carried out in Cadence Virtuoso using the GPDK045 45 nm process. Layout of proposed circuit is shown in Fig.11.The following figures cover all key performance

metrics: input matching (S_{11}), noise figure, power gain (S_{21}), and linearity (IIP3) with and without the post-distortion transistor M_{pd}.

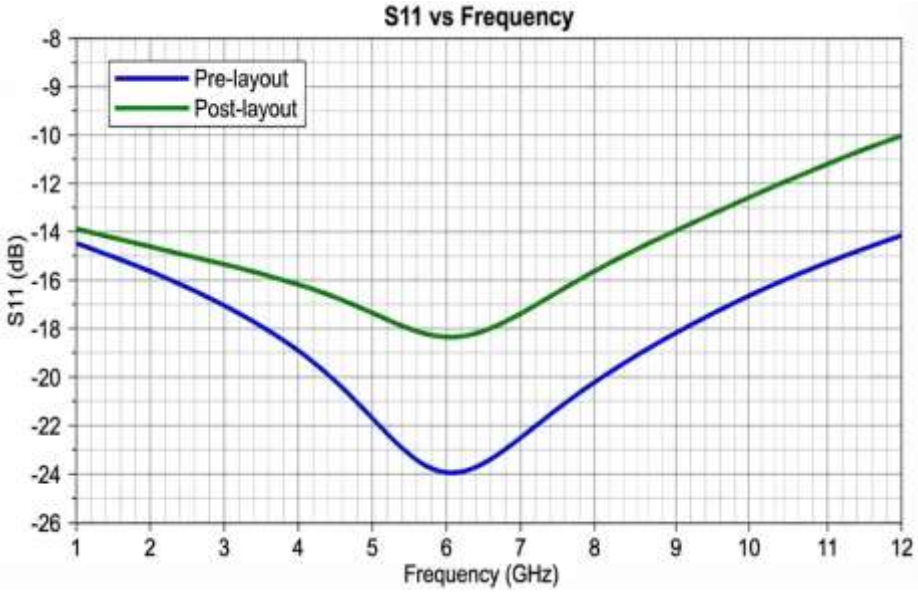

Fig.5. Input impedance S_{11} (Pre and post layout simulation)

Fig. 5 shows the simulated S_{11} across 1–12 GHz for both pre-layout and post-layout conditions. S_{11}remains below −10 dB across the entire UWB band in both cases, confirming that the addition of M_{pd} does not perturb the broadband input matching. The post-layout result exhibits a slight frequency shift due to parasitic routing inductance and capacitance, which was accounted for by re-tuning L_{in}. The wideband matching is maintained by the active feedforward G_m-boosting network, which effectively increases the input transconductance without raising bias current.

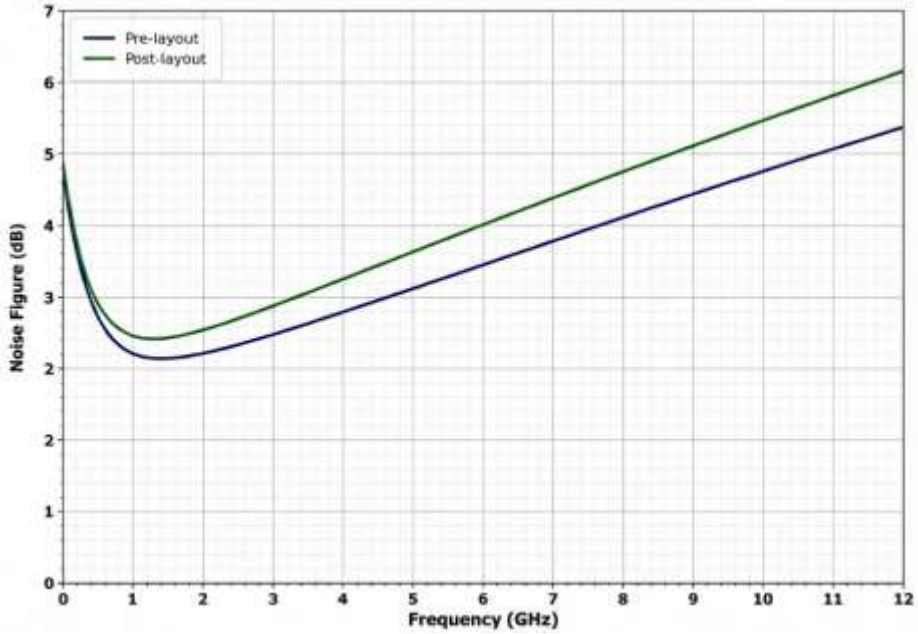

Fig. 6. Noise Figure — Pre- and post-layout simulation

Fig. 6 shows the simulated NF across 1–12 GHz. In pre-layout simulation the NF ranges from 2.2 dB to 5.3 dB. Post-layout extraction raises the NF slightly to the 2.8–6.1 dB range, owing to parasitic metal resistance and reduced inductor Q-factor. This result confirms that M_{pd} adds negligible noise, consistent with the theoretical prediction of Section 3.2.3 where the noise from M_{pd} is suppressed by N^2 in the denominator of equation (20).

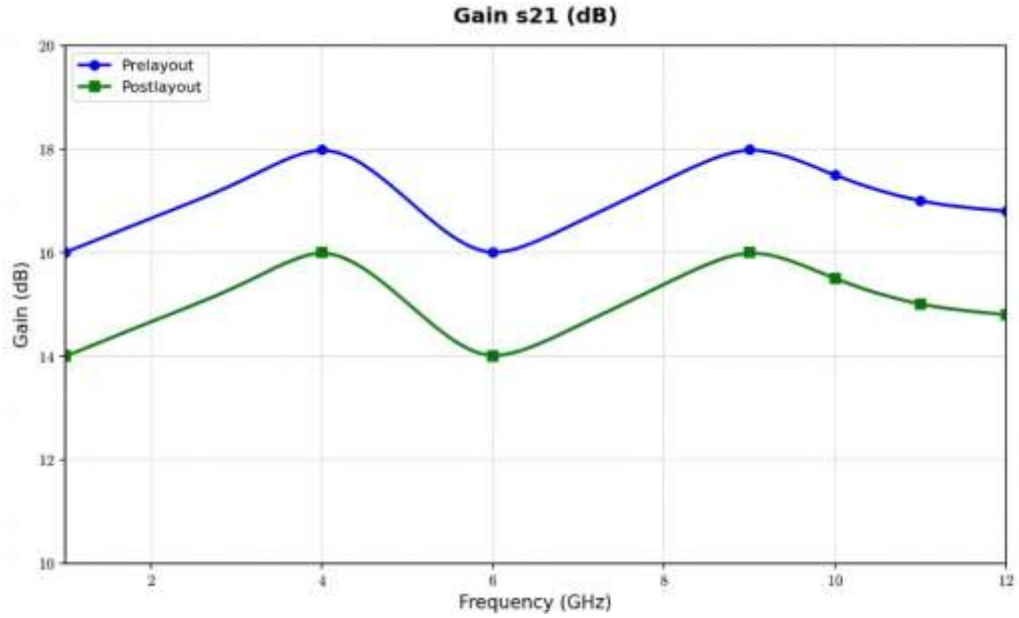

Fig.7. Gain S_{21} (Pre and post layout simulation)

Fig. 7 presents the simulated power gain S_{21}. The pre-layout peak gain reaches approximately 18 dB, consistent with the analytical expression in equation (2). Post-layout gain is slightly reduced, again due to parasitic losses in routing and passive components. The gain-flatness across the 1–12 GHz band is maintained in both conditions, confirming that M_{pd} introduces no meaningful gain degradation.

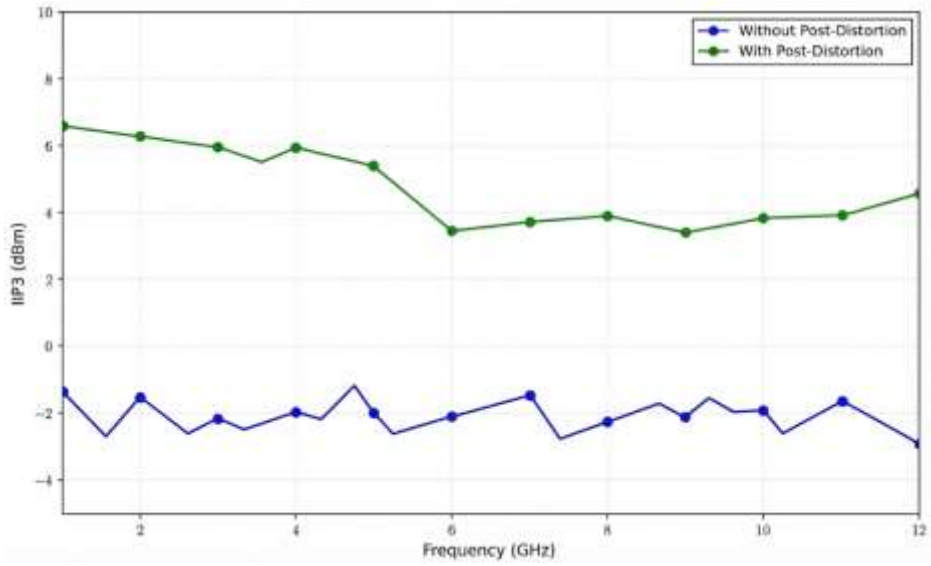

Fig.8. IIP_3 (with and without Post distortion transistor- Pre-layout simulation)

Fig. 8 directly compares the IIP3 with and without M_{pd} from pre-layout simulation. The pre-layout simulation in GPDK045 by enabling M_{pd} and setting V_{PD} to the analytically derived optimum from equation (67), the IIP3 improves substantially, confirming that the positive G_{m3Mpd} from M_{pd} effectively offsets the negative G_{m3M2} from M_2, as predicted by the distortion analysis in Section 3.3.
The two-tone test confirms that the positive G_{m3Mpd} current from M_{pd} directly opposes the compressive G_{m3M2} from M_2, in line with the analytical cancellation condition of equation (64).

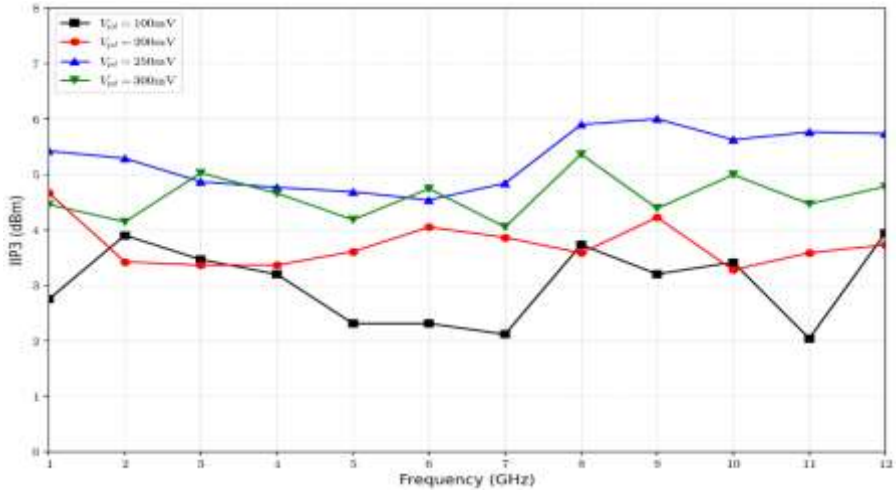

Fig.9. Variation of IIP_3 with V_{PD} (Pre-layout simulation)

Fig. 9 plots the simulated IIP3 as a function of the bias voltage V_{PD}. A clear peak in IIP3 is observed at the optimal V_{PD} value, corresponding to the condition G_{m3} total $\rightarrow 0$ derived in equation (64). Away from this optimum, IIP3 decreases monotonically in both directions as the partial cancellation degrades. The sharpness of this peak reflects the exponential sensitivity of $g''_{m,pd}$ to V_{PD}, as expressed in equation (66). This tuning characteristic enables the circuit to be digitally trimmed post-fabrication, compensating for process and temperature variations.

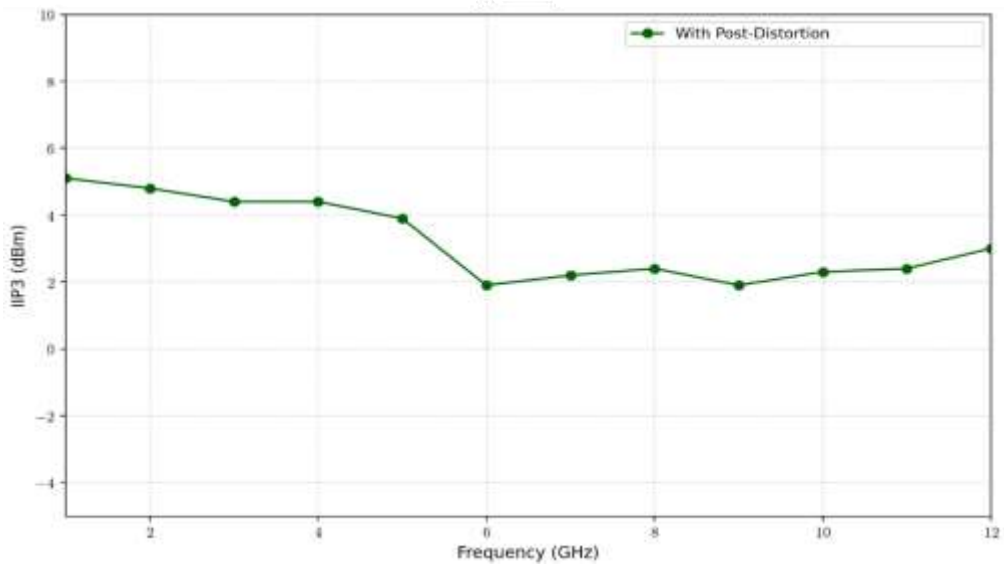

Fig.10. IIP_3 (post layout simulation)

Fig. 10 presents the post-layout IIP3 simulation. The IIP3 improvement is maintained after parasitic extraction, confirming the robustness of the post-distortion approach to layout-induced parasitics. The post-layout IIP3 is slightly lower than the pre-layout value due to additional parasitic capacitance at node S from routing and well diffusions, which partially modifies the effective β and shifts the optimal V_{PD} slightly from its pre-layout value. Re-tuning V_{PD} in the post-layout case restores the IIP_3 improvement.

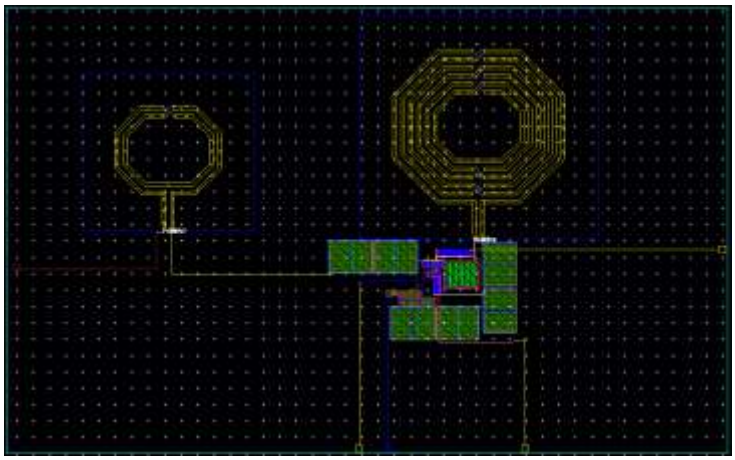

Fig. 11. Layout of the proposed LNA

5. Comparison with Prior Art

Table 3 benchmarks the proposed design against the proposed LNA in [1] and selected previously published wideband LNAs. The proposed LNA in [1] set an excellent reference in terms of gain, NF, bandwidth, power, and area using 40 nm CMOS. Blaakmeer et al. [9] established the foundational CG-CS balun-LNA with simultaneous noise and distortion cancellation at higher power. Kim et al. [13] combined G_m-boosting with balanced loads for low-power operation. Chen et al. [16] achieved IIP3 of +3 dBm through combined noise and distortion cancellation at higher power cost. Shirmohammadi et al. [18] used post-distortion with derivative superposition and weak-inversion transistors in a balun-LNA, obtaining a 5.22 dB IIP3 improvement with only 95 µA of extra current.

The proposed circuit delivers IIP3 improvement through a single M_{pd} transistor in weak inversion, retaining all merits of [1] including the dual noise and distortion cancellation of M_{1n} and M_{3n}, current reduction via active feedforward, and compact die area. The IIP3 improvement factor over [1] is:

$$\frac{IIP3_{proposed}}{IIP3_{Fig.1}} = \sqrt{\left|\frac{G_{m3,Fig.1}}{G_{m3,Fig.1} - G_{m3,pd}}\right|} \quad \text{..... (69)}$$

As G_{m3Mpd} approaches $G_{m3,base}$ through tuning V_{pd}, this ratio approaches infinity—confirming that theoretically unlimited IIP3 is achievable at the optimal bias condition.

Table 3. Performance Comparison with Previously Published Wideband LNAs

Reference	BW (GHz)	Gain (dB)	NF (dB)	IIP3 (dBm)	PDC (mW)	Area (mm^2)	Technique
[1] Liu 2021	1–11	17	3.5-5.5	−2.8@6G	9	0.061	AF+NC+CM

[9] Blaakmeer 2008	0.1–6	11.5	2.6	+6.3	20	N/A	NC+Balun
[13] Kim 2020	0.05–2	18.7	2.3	−12	5.5	0.19	Gm-boost+NC
[16] Chen 2008	0.2–5.2	16	2–3	+3	20	N/A	NC+DC
[18] Shirmohammadi 2022	0.47–3.3	22	2.57	+2.81	12.5	0.057	PD+DS(WI)
This Work (GPDK045)	1–12	16	2.8–6.1	+5	12.8	0.082	AF+NC+PD-WI

AF: Active Feedforward; NC: Noise Cancellation; CM: Current Mirror; DC: Distortion Cancellation; PD: Post-Distortion; DS: Derivative Superposition; WI: Weak Inversion.

6. Conclusion

A linearity-enhanced wideband CMOS LNA implemented in 45 nm GPDK045 using Cadence Virtuoso has been presented. The design extends the active feedforward noise-cancellation architecture of [1] through the addition of a single post-distortion transistor M_{pd} in the subthreshold region. The circuit in Fig.1 uses M_{3n} and R_3 as an active feedforward G_m-boost stage in the main path, bringing the CG transistor current below 1 mA and reducing the dominant M_4 noise contribution. The NC condition $N = g_{m2}R_s$ theoretically nulls the noise from both M_{1n} and the G_m-boost stage M_{3n} at the output.

The proposed M_{pd}, with gate at node Q and drain at output node S, operates in the subthreshold region and develops a positive third-order transconductance derivative $g''_{m,pd} > 0$ from its exponential I-V characteristic. A complete third-order Taylor-series nonlinear analysis was performed, extending the KCL and power-series derivation to include i_{pd}. After applying NC condition $N = g_{m2}R_s$ and input matching condition $b_1 = \frac{1}{2}$, the simplified output current in equations (54)–(57) was derived. The IIP3 expression (equations 61–62) shows that the positive G_{m3Mpd} from M_{pd} offsets the negative G_{m3M2} from M_2, driving the total third-order coefficient G_m-total toward zero and greatly improving IIP3.

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