

An Overview of Vedic Mathematics Sutras with Application

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Abstract:

The aim of the paper highlights the versatility and efficacy of vedic mathematics Sutras through real-world applications. Vedic mathematics is an ancient Indian mathematical system that comprises 16 sutras and 13 sub-sutras. These sutras find applications in various fields such as computer science, number systems, cryptography, microcontrollers, digital signals, filters, and more. This study compares and summarizes some important sutras from vedic mathematics with their recent applications.

Keywords: Vedic Mathematics, Cryptology, Filters, Multipliers and Microcontrollers.

I. INTRODUCTION

The Vedas, which are considered holy scriptures in India, are described as "knowledge, insight, and sacred writings" in Sanskrit. The sixteen elementary mathematical sutras from the Vedas, were recomposed by the Jagadguru Sankaracarya Sri Bharati Krisna Tirthaji Maharaja [14]. These sutras are majorly mental calculation based and used for faster calculation with accuracy. Each of the sixteen formulas touches a distinct area of mathematics. These sixteen sutras are used to answer the problems of arithmetic, algebra, geometry, calculus, trigonometry in faster way. These sutras are so precisely connected that using one sutra problems of different aspects can be solved. Using the vedic sutras for various real-world applications can lead to the well performed systems.

Researchers are working on implementing vedic sutra-based calculations in various fields in order to increase their efficiency and reduce processing time. These fields include Microcontroller, Digital Signal Processor (DSP), Multipliers, Cryptosystem, Filters and many more. In this paper vedic sutra-based system is compared with traditional system in terms of time, area, power, efficiency and accuracy [6,10]. Microcontroller used in industrial processor, mobiles using logical computation. With use of vedic sutras a set of complicated calculation can be avoided and efficiency of its processor can be increased. Vedic sutra-based microcontroller can replace the use of DSP [9, 18]. Using vedic sutras, more efficient DSP can also be made.

Gaikwad et al. [5] (2015) and Lisa et al. [13] (2018) presented review papers on implementation of vedic sutra in DSPs to improve speed. Their review works were related to explain implementation of Urdhva-Tiryagbhyam sutra and to analyze computational complexity. Biji et al. [3] used Urdhva-Tiryagbhyam, Nikhilam and Dhvajank sutras for multiplication and division algorithms in DSP and compared them with conventional method. Using vedic sutras highly efficient Discrete Fourier Transforms (DFT) and Fast Fourier Transforms (FFT) are also introduced [1,2,20].

Using Urdhva-Tiryagbhyam, Nikhilam, Dvandva-Yoga and Anurupya sutra in multipliers resulted in more efficient and faster multiplier involving less error. Accurate squarer and cuber are obtained with very few

steps [8,17,21]. Vedic sutras are also applied to the cumbersome calculations of cryptosystem. Jose et al. [7] used vedic sutras to implement RSA system and compared it with conventional method. Its positive result in terms of saving time with less error attracted attention of many researchers. The implementation of vedic sutras for the computation of RSA encryption/decryption, saved resources and processing time [12,19].

Application of vedic sutras in filters resulted more efficient and reduced computational system comparative to the traditional system. To carry out the reduced computation in filter, Urdhva-Tiryagbhyam sutra is implied [4,15]. Using Urdhva-Tiryagbhyam and Nikhilam sutra, 32-bit and 64-bit IIR filter is obtained with faster speed and higher accuracy [11,16]. Application and Implementation of vedic sutras is also seen in computer architecture. This review paper contributes to the deeper understanding of vedic sutras and its relevance to the real-life application.

This paper is organized as, In Section II, the paper introduces some vedic mathematics sutras. In Section III, the application fields of vedic mathematics are explained. Section IV, deals with the major finding of some of the researchers who have already done work on implementation of vedic sutras and in Section V includes the conclusion.

II. APPLIED VEDIC SUTRAS

The vedic sutras used for the given real-world applications are as follows.

2.1 Urdhva-Tiryagbhyam Sutra

Urdhva-Tiryagbhyam sutra is the most capable of being used for multiplication and as well as for division. Figure 1 is used to explain the multiplication method of Urdhva-Tiryagbhyam sutra. It shows how to multiply two 3-digit values, $a_2a_1a_0$ and $b_2b_1b_0$. Computing the sum of the partial products, a_0b_0 , $a_1b_0 + a_0b_1$, $a_2b_0 + a_1b_1 + a_0b_2$, $a_2b_1 + a_1b_2$, a_2b_2 , is the first step. Shifting the carry from right to left is the second stage.

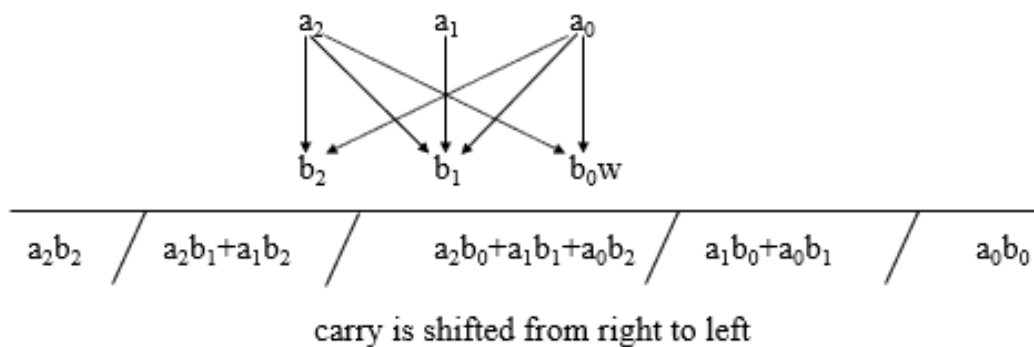


Figure 1: Multiplication of 3-digit numbers using Urdhva-Tiryagbhyam Sutra

2.2 Nikhilam Sutra

Nikhilam sutra translates as "all from 9 and the last from 10". In vedic mathematics, the Nikhilam Sutra introduces methods for multiplication and division of numbers speedily. For the product of n -digit numbers a and b , having base 10^n and x, y be the vinculum of a, b respectively, is expressed as $a \times b = (10^n - x) \times (10^n - y) = 10^n(10^n - x - y) + xy$.

2.3 Anurupyena Sutra

The Anurupyena Sutra is an upasutra. Applying this actually means that the ratio should always be taken

into consideration and should result in a proportionate multiplication or division, depending on the situation, whenever there is a ratio-wise relationship between proportions.

2.4 Dvandva Yoga Sutra

In Dvandva-Yoga sutra the fundamental unit known as 'Dvandva', used to determine the square of a number, is calculated in different ways. Using D for the denotation of Dvandva. Hence, Dvandva can be defined as follows

$$D(a) = a^2$$

$$D(ab) = 2 \times a \times b$$

$$D(abc) = 2 \times a \times c + b^2 \text{ and so on.}$$

2.5 Dhvajank Sutra

A division method known as the “Dhwajank Sutra” divides the divisor into two parts. The term “Dhwajank” refers to the right part, and “principal divisor” refers to the left. The principal divisor and the Dhvajank are both placed in the divisor section, and only the principal divisor is used for the division.

2.6 Anurupya Sutra

The Anurupya sutra is used to calculate the cube of any two-digit number. The suggested method utilizes the concepts of the Urdhva-Tiryagbhyam sutra for multiplication. Figure 2 illustrate the Anurupya sutra. The procedure to calculate the cube of 2-digit number xy, where x is the ten’s digit and y is one’s digit number, is as follows.

$$\begin{array}{r}
 (xy)^3 = \quad + \quad \begin{array}{cccc} x^3 & x^2y & xy^2 & y^3 \\ & 2x^2y & 2xy^2 & \end{array} \\
 \hline
 x^3 + 3x^2y + 3xy^2 + y^3 \\
 \hline
 \end{array}$$

Figure 2: Cube of a number using Anurupya Sutra

III. APPLIED AREAS OF VEDIC SUTRAS

Vedic sutras are the important aspect of mathematics that has practical application in various fields. The idea of using vedic sutras can be adapted to these applications to make them faster and more efficient.

3.1 Microcontroller

A microcontroller is a tiny integrated circuit that is used in embedded systems to control particular functions. It is a compressed microcomputer designed to manage embedded systems in various devices such as cars, office equipment, robotics, home appliances, and transportation. To perform all these functions microcontroller requires a complicated set of calculations. This set of calculation may limit the speed of microcontrollers. By using DSPs always offers the possibility of better performance, but raises project costs and system complexity. This is when the vedic Mathematics becomes relevant. Simplified calculations can greatly enhance the controller's processing speed and performance. Using logical calculations grounded in vedic mathematics sutras this aim is achieved. The sutras of vedic mathematics contain the logics required for these computations, which can be easily incorporated into an application and created as a code. These codes are used directly when the calculation is needed. The controller chooses the procedure based on a logical choice. Reddy from Interleaved Technologies, Hyderabad, observed and concluded that to create an answer for a code on an 8051 series, using vedic sutra based microcontroller up to ten or fifteen times the initial speed can be achieved as compared to convenient microcontroller. As a result, DSP based microcontrollers become practically unnecessary.

Using these vedic sutra-based microcontroller for various real-world application. These applications based on vedic sutras consumes less power and less time, hence gives contribution to

3.1.1 Aerofoil Controllers

Aerofoil is a collection of number of sensors that collect and transmit data to the laptop, where calculations are performed and the required inclination is transmitted back to the activators. The plan is to modify computation performance and decrease processing time by implementing vedic sutras.

3.1.2 Mobile Application

Android apps need to be effective in order to avoid interfering with phone calls. Although android devices have been modified a lot, such as if the factorial of a number is to find using scientific calculator in an android device, it is going to take nearly a second. This is where vedic mathematics' logical computations can be applied to change the code and accelerate processing.

3.1.3 Transformer Winding Machines

Transformer winding machines are typically equipped with data input devices that receive parameters such as code, bobbin, primary and secondary number of turns and gauge. Since, it is possible here to program an 8051 microcontroller to automate transformer winding. By increasing speed of microcontrollers, the efficiency of transformer winding machines can be enhanced.

3.2 Digital Signals Processors

DSP digitize and statistically alter real-world signals. It is made to quickly execute mathematical algebraic operations for the enhancement of digital communication's accuracy and reliability. The focus of DSP is a significant area of electronics and telecommunications engineering. Multiplication is crucial for the design of DSP operations because it allows signal processing operations like correlation and convolution to be performed. For short sequences, the new implementation strategy is must, to make DSP operations cognitively and easily calculable.

A DSP operating method based on vedic sutras can be considered. Using the vedic Urdhava-Triyagbhayam multiplication sutra, high speed DSP operations of two finite length sequences can be performed. In research by Akhalesh et al.[1], MATLAB is used to build vedic multiplier, and a single Graphical User Interface (GUI) window is used for all operations. When compared to MATLAB's built-in functions, vedic sutra-based DSP operations minimized processing time and cuts down internal functions by 40–60%.

In digital signal processing and image processing, the convolution is essential. It is employed in the creation of correlation applications and digital filters. The linear convolution uses a basic vedic multiplier to successfully construct. The basic concept of convolution is used to construct fourier transform.

3.2.1 Discrete Fourier Transform

The DFT is frequently used in digital signal and image processing applications. It allows data to be converted from the time domain to the frequency domain. The application of the DFT system using both conventional method and vedic sutra method is examined and analysed. It is proposed that adapting the entire computer system at the architectural level to the vedic sutra method improves the DFT procedure's overall efficiency.

3.2.2 Fast Fourier Transform

FFT is an efficient method that uses fewer computations than direct DFT evaluation. The FFT minimizes the direct computations required for the iterative calculation of the DFT coefficients. When compared to direct evaluation of the DFT, FFT improves performance by a factor of 100 or more and decreases the calculation time needed to construct a DFT. According to the Aksata et al.[2], by using vedic multipliers

in FFT designed in Verilog, the 8-bit array multiplier has a time delay of 88.967 ns; the 8-bit booth multiplier has a time delay of 46.733 ns; the 8-bit vedic multiplier by Urdhva-Tiryakbhyam method has a time delay of 44.507 ns; and the 8-bit vedic multiplier by Nikhilam method has a time delay of 18.134 ns. The time delays for the 16-bit array multiplier, 16-bit booth multiplier, 16-bit vedic multiplier using Urdhva-Tiryagbhyam, and 16-bit vedic multiplier using Nikhilam are likewise 86.130 ns, 64.343 ns, and 20.72 ns, respectively. Furthermore, the FFT design time delay is as follows: 58.553 ns for the FFT using an array multiplier, 49.33 ns for the FFT using a booth multiplier, 42.403 ns for the FFT using the Urdhva-Tiryagbhyam Method, and 13.928 ns for the FFT using the Nikhilam Method.

3.3 Multipliers

In most applications involving DSP, multiplication is a fundamental operation. The processing speed of a processor's DSP is defined by its multiplier. Creating an efficient multiplier contributes to enhanced microprocessor, system performance and efficient DSP. Considering the fact that multipliers are the primary components used in CPU activities, vedic mathematics is used for faster multiplication operations. This approach typically results in reduced processor area, power consumption, and delay. Since, the vedic multiplier with the use of sutra Urdhva-Tiryagbhyam and sutra Nikhilam, have superseded the traditional multiplier method. These multipliers were created and described in Verilog Hardware Description Language(HDL). The parameters for 32, 64, and 128 binary bit multiplication were compared, including delay time, area (number of sliced Look Up Tables-LUTs and number of bonded Input Output Bonds-IOBs), and power.

Out of 16 sutras of vedic mathematics only the Nikhilam sutra and the Urdhva-Tiryagbhyam sutra are most suitable for multiplication. Nikhilam sutra makes multiplication easier for integers that are closer to powers of 10, whereas the Urdhva-Tiryagbhyam sutra is a broad method that does not place limits on the multiplier or multiplicand's numerical values. Due to its general nature, it is the most potent method of vedic multiplication.

On a comparison made by Vitthal et al.[21], it is observed that vedic multipliers always use much less space and consume more power than Array multipliers of the same bit-width. Vedic multipliers have lower time delay. Overall, the vedic multipliers outperform the conventional Array Multipliers.

3.3.1 Squarer

Squarers for the processor can be made by using different methods. But by using vedic sutra for making squarer area, time and power consumption can be reduced. When using the vedic Squarer instead of array multipliers to accomplish the square operation, area and power savings can reach up to 63.63% and 74.47%, respectively. Delay is minimized up to 72.036%. Squarer based on Dvandva Yoga can be the best option to replace with Array squarer. The calculation method of Dvandva Yoga based squarer appear to be similar to Urdhva-Tiryagbhyam sutra. Any of the method can be used here. Vedic squarer uses less resources results in circuit's less power and time delay. The results section's facts provide validity to this conclusion.

3.3.2 Cuber

Vedic mathematics based cuber system can be made using Anurupya Sutra. Anurupya based cuber can be the replacement of tradition cuber as it reduces computation and increases accuracy. Area savings up to 98.92%, power reductions up to 99.14%, and delay reductions up to 96.529% can be achieved using vedic cuber.

3.4 RSA Cryptosystem

The term "cryptography" in computer science refers to safe information and communication methods that use mathematical concepts and a series of computations. This computation is used to change messages into forms that are difficult to interpret. Rivest Shamir Adleman (RSA) is a popular asymmetric cryptography system. This system develops a private and public key combination for encryption and decryption, which safeguards sensitive data. Data is encrypted and decrypted by using the safe cryptographic system RSA. The RSA system can be simplified in few easy steps.

Encryption is described as $C = Pe \pmod{n}$ (1)

Decryption is described as $P = Cd \pmod{n}$ (2)

This system's hardware version often operates more quickly than its software. Still, its performance can be enhanced by using vedic sutras. The computation of $Pe \pmod{n}$, where P is the text and (e, n) is the pub key, is one of the most time-consuming steps in the RSA encryption/decryption system. For RSA system to function at the same speed as its software, it requires a fast division and a fast modular multiplication method. This is where vedic sutras can be implemented.

Jose et al.[7] concluded that, the speed, power consumption, and space utilization of the RSA system are enhanced when vedic division method is used. The speed of the system is accelerated by the vedic multiplication at the instant where the hardware and software are operated simultaneously.

The sutras contained in the ancient vedic mathematics can be used to simplify RSA system faster. Such as Urdhva-Tiryagbhyam and Nikhilam Sutra for vedic multipliers, Dhwanada Yoga method for vedic squarer and for vedic division Dhvajank method can be used. Improved speed and area efficiency is noted in the vedic method-based RSA system. Its gate delay and area rise comparatively slows down with increasing bit count, as compared to RSA system that uses traditional multipliers and division methods.

3.5 Filters

A filter is a circuit that may reduce certain frequencies while allowing others to flow through. As a result, crucial frequencies can be separated from unwanted frequencies in signals using a filter. A digital filter uses mathematical computations for the signal's sampled values. These mathematical computations demand numerous steps in conventional methods while vedic sutras helps to find solutions in one or a few steps. Multiplication, divisibility, complex numbers, squaring, cubing, and square and cube roots are all made easier and simpler by vedic mathematics.

The appearance of the filter in the time domain is referred to as the "Impulse Response." Digital filter can be classified as finite impulse response (FIR) and infinite impulse response (IIR).

3.5.1 Finite Impulse Response

On DSP systems, digital FIR filtering is a very potent process. For the past few decades, many of the FIR filter problems were due to large and complicated multiplication. As a result, the traditional FIR filter requires over power consumption, large area and latency. This issue is resolved by using vedic multipliers in FIR filters.

Pasuluri et al. [15] presented a modified Nikhilam multiplier based 8-tap FIR filter and concluded the decrement in delay and increment in efficiency. The findings indicate that the current architecture has a 20% faster processing speed than the FIR filter in use. Additionally, the vedic multiplier-based FIR filter uses around 50% less power and 30% less space than the traditional FIR filter based on array multipliers. Chaturvedi et al. [4] showed that using vedic multiplication sutra Urdhva-Tiryagbhyam in GUI window, the FIR filter takes less processing time on an average than inbuilt MATLAB function.

3.5.2 Infinite Impulse Response

The IIR filtering process is one of the most significant DSP operations. IIR filters are recursive digital filters. Compared to FIR filters of the same order, IIR filters have a far superior frequency response. Kunthe et al.[11] used the Urdhava-Triyagbhayam sutra to construct the IIR filter. This algorithm is run through a GUI in MATLAB. On comparing the IIR filter based on Urdhva-Tiryagbhyam sutra to MATLAB's built-in function, processing time is reduced. IIR filter based on vedic approach requires lesser processing time on an average. Despite its widespread recognition, DSP processor based on vedic mathematics have not employed much. Savadi et al. [16] used IIR filter based on the Urdhava-Triyagbhayam sutra. This computation was carried out on a vertex-5 FPGA (XC5VLX50T+1136) using Xilinx 13.4 ISE. This vedic sutra based IIR filter required less processing time on an average, as compared to traditional methods.

IV. RESULTS AND DISCUSSION

From the reviews of various papers, we got many major findings. Many researchers applied vedic sutras for different fields and also succeeded to reduce time delay, power consumption, area in utilization and observed higher accuracy. Results for different application using vedic mathematics, of few of them are discussed below:

Table 4.1 Results for different application

S.No	Author of the paper	Application fields of vedic sutras	Results of using vedic sutras
1	Akhalesh et al. [1]	Digital Signal Processing	Decreased internal functions and so processing time.
2	Aksata et al. [2]	Applied for FFT design	Highly efficient in terms of time delay.
3	Chaturvedi et al. [4]	Applied for higher order FIR filter	Higher performance and quality with decreased processing time.
4	Joze et al. [7]	Applied of RSA Cryptosystem	Improved speed, power and in area utilization.
5	Kunthe et al. [11]	For 32 order IIR filter design	Higher performance and quality consuming less average time.
6	Pasuluri et al. [15]	Applied for 8 order FIR filter	Higher processing speed, less power consumption and less area utilization
7	Savadi et al. [16]	Applied for 64-bit IIR filter	More effective and faster than customary method.
8	Sundaram et al. [18]	For ALU computations	Reducing time delay and area and lowering circuit complexity.
9	Vitthal et al. [21]	Applied for Multipliers, squarer and cuber	There is a lot of room to improve how well current mathematical operations can be operated with less time delay.

V. CONCLUSION

The presented paper reviewed the vedic sutra-based microcontroller, vedic multiplier and observed their implementation on DSP, filters and in cryptosystem. In this paper the vedic sutra-based systems are compared with traditional systems. These systems involved many algebraic operations like multiplication, division, squaring and cubing. From the above observations and reviews, it is concluded that using vedic sutras in the given real-life application, increases accuracy and decreases time delay, computational steps. The most captivating result is, it can be estimated that the calculation method used in vedic era were more simplified, accurate, faster and mainly mental calculation based. Therefore, this paper makes an important contribution to the ongoing study on relevance of vedic sutras on real-life application and leaves a scope for improvement in the efficiency of present systems.

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