International Journal for Multidisciplinary Research (IJFMR)
E-ISSN: 2582-2160 ● Website: www.ijfmr.com ● Email: editor@ijfmr.com

Emerging Trends in Low Power VLSI Architecture for WSN Application- An Overview

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Abstract
Wireless sensor network (WSN) is an emerging field which demands an energy efficient ultra-low power VLSI architecture which delivers high performance with less power consumption as most of the sensor nodes are battery operated. An innovative architecture need to be designed which demonstrates circuit level leakage reduction technique with power optimization and complete ASIC implementation for WSN application. There are various techniques such as transistor stacking, MTCMOS, power gating, clock gating, DVFS which are individually used for power optimization. The main aim of this paper is perform a comprehensive study on the works that are been carried out reduce overall power consumption and integrating it with a complete ASIC flow for PPA optimization.

Keywords: Low Power VLSI(Very Large Scale Integration) Design, Wireless Sensor Network , ASIC (Application Specific Integrated Circuits) Implementation, PPA (Power Performance Area) Optimization.

1. Introduction

Wireless Sensor networks is a fast growing field that has infinite number of application such as weather monitoring, health care application, industrial automation and structural health , smart agriculture, home automation etc. The architecture consists of sensor nodes, gateway, internet and user node. Sensor nodes are randomly distributed network as shown in Figure 1. These networks consist of a small interconnecting device that are used to monitor, collect data, process data, and communicate it to the centralized base station for data analysis.

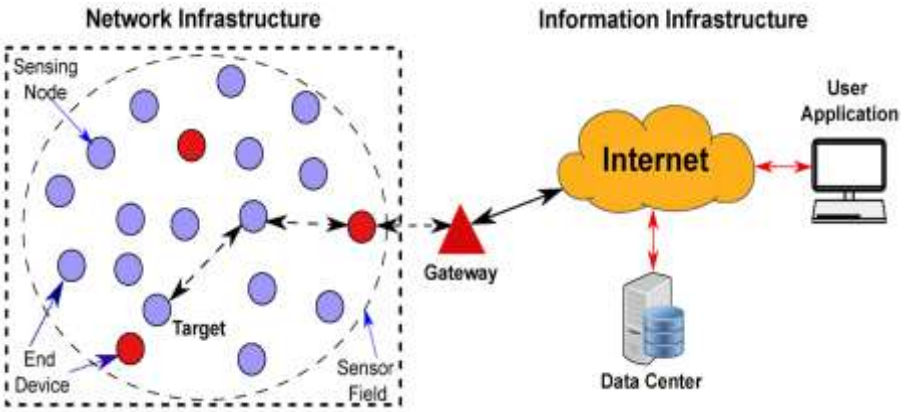

Figure 1. Architecture of WSN

These sensor nodes are usually battery operated and works on a coin cell battery, sensor nodes are in sleep mode; wake up only when they needed to sense the data, process and communicate through gateway to end user. This process consumes highest rate of power, as the power consumption increase, the sensor nodes enter into idle state giving rise to static power consumption, which contributes to overall power consumption. This lead to the need for low power VLSI architecture. There by reducing static power and dynamic power is most important to extend the battery life.

The technique such as clock gating, dynamic voltage and frequency scaling are used for reduction of dynamic power consumption [2,3] and power gating, multi-threshold CMOS, transistor stacking are used for reduction of static power consumption[1,4]. These techniques can be integrated into a complete ASIC design flow for a better power optimization.

The existing processors in WSN utilize more power for data handling, there by RISC-V processor with modular instruction set architecture (ISA)[18] allows the design to design an application specific integrated circuit which can simultaneously reduce both static and dynamic power without effecting the performance and area parameters.

2. Literature Review

WSN are usually deployed in remote areas and are usually operated on coil cell battery , due to the continuous usage if sensory nodes for sensing and collecting of data power consumption is more leading to reduction of battery life this is when low power architecture plays an important role to reduce power at circuit level, architecture level and system level.

Initially WSN was designed using microcontrollers as it was easy to implement but it has high power consumption due to switching activity of clock hence researcher shifted to SoC, which improved the performance and lower the power consumption. In SoC design, dynamic power was the primary source of power consumption but as the CMOS technology dropped to submicron or nanometer, leakage power was a significant source of power dissipation hence various technique such as clock gating, Dynamic Voltage and Frequency Scaling (DVFS), power gating, Mutli-Threshold CMOS (MTCMOS), transistor stacking were used to reduce both dynamic and static power respectively.

Author in [1] explains about increase of sub threshold leakage, gate oxide leakage, junction leakage as CMOS technology scales down and suggest the usage of transistor stacking, MTCMOS, sleep transistor methods for reduction of leakage current.

Author [3] introduces the concept of modified feedback sleeper stack technique by combining a sleep transistor with feedback control to reduce leakage power; he uses the concept of high V^{th} and dual V_{sub} and validates the process through circuit level.

Author in [4] demonstrated the reduction of dynamic power using clock gating on pipelined RISC-V architecture and showed that a reduction of up to 57% can be obtained using single cycle and up to 23% in pipelined architecture and suggested that by combining reduction technique static power can also be reduced.

Author in [5] presented a comparative analysis of different techniques for static power reduction such as transistor stacking, MTCMOS, sleepy keeper and power gating on a NAND gate and concluded each technique offers different tradeoff between leakage, power, performance and area and no individual method is suitable for all applications of WSN hence a customized hybrid model need to be designed to achieve Power Performance Area (PPA) optimization.

Further improvement level at processor architecture level was reported by author in [6], who investigates power optimization throughout Application Specific Integrated Circuit (ASIC) and physical design stages of RISC-V and shows that optimization of physical design will significantly reduce power without modifying the processor it highlights the importance of Electronic Design Automation (EDA) tools in achieving low power ASIC implementation

The paper [7] proposes a power optimization model for WSN using FPGA by using clock management technique for static reduction, this improves energy efficiency but limits its application to low power commercial sensors as FPGA consumes more power the author suggests a custom ASIC implementation for efficient PPA optimization.

The author in [8] proposes an architecture using RISC-V based PicoSoc for instruction aware clock gating mechanism which selectively enables the clock module by decoding the instruction and hence reduces unwanted switching activity which in turn reduces dynamic power without effecting performance and area.

The paper [9] describes a hybrid model for MTCMOS technique to reduce static leakage power by combining transistor stacking with MTCMOS and demonstrate theoretically the reduction of leakage power by maintaining performance and area.

Binding power reduction technique and Artificial Intelligence (AI) to drive automation for low power IC by introducing machine learning algorithm for PPA puts lights on emerging trends of AI into Electronic Design Automation (EDA) workflow [10].

3. Limitation and Prospects

A considerable amount of progress has been made in the field of low power VLSI design for WSN application. There are wide range of technique for power reduction such as transistor stacking, MTCMOS, power gating, clock gating have shown a significant improvement in leakage power depending on the application and design.

Many research focus on single level optimization, circuit level approach which focus on reduced switching activity. Only few studies have combined both approaches which can address both dynamic and static power consumption. Secondly growth in field of RISC-V opens new opportunity for WSN application focusing on optimization, leakage reduction.

Another gap identified is use of FPGA platform for validation of low power [5,12] it consumes more power hence customized ASIC implementation would be a better choice for more reliable power reduction and system efficiency. Recent advances have introduced AI into EDA to improve design area and power optimization. There is a considerable scope for more exploration in AI based low power design methodology.

4. Conclusion

There are several optimization techniques which are used for significant reduction of dynamic and static power, they are individual parameters which are optimized separately but by combining transistor stacking, multi-thread CMOS methods together power optimization would be better, VLSI architectures are validated through RTL to GDSII flow for silicon-oriented Power-Performance-Area optimization.

5. Acknowledgement

We would like to thank Mr. Chandramohan. U, Founder CTO, Banashree SemiConductors, for his conti-

nuous encouragement and support to carry out this review work.

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